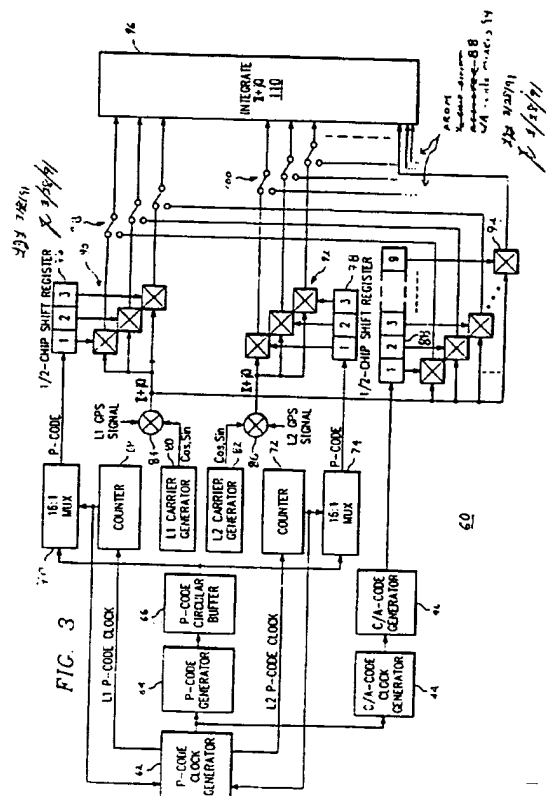


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**71 Applicant : TEXAS INSTRUMENTS  
INCORPORATED  
13500 North Central Expressway  
Dallas Texas 75265 (US)**

**(74) Representative : Nettleton, John Victor et al**  
**Abel & Imray Northumberland House 303-306**  
**High Holborn**  
**London, WC1V 7LH (GB)**

57 An enhanced P-code channel (60) for use in a GPS receiver (10) to simultaneously track L1 and L2 comprises a P-code clock generator (62) for generating two code clocks. The first code clock associates with L1 and the second associates with L2. The code clocks have the same frequency but different phases from one another. Circuitry (64) and (66) generate and store a plurality of P-code chips. A first circuit (68, 70) selects and updates P-code chips from the stored P-code chips that are in phase with the L1 code clock. A second circuit (72 and 74) selects and updates P-code chips from the P-code chips and phased with the L2 code clock.



## TECHNICAL FIELD OF THE INVENTION

This invention relates to Global Positioning System (GPS) receivers and more particularly a method for enhancing an a single receiver channel for processing a plurality of L-band signals.

## BACKGROUND OF THE INVENTION

The NAVSTAR Global Positioning System (GPS) is used to determine exact geographic position (i.e. latitude, longitude, and height above the earth) as well as the exact velocity and time of stationary or moving objects. The navigation receiver calculates position, and time by determining distance to a series of satellites. The navigation receiver calculates velocity by determining doppler frequency shift of the satellite signals.

The NAVSTAR GPS receiver must receive signals generated from the satellite about 11,000 miles away. Each GPS satellite transmits a 6-watt signal. The satellite and receiver, therefore, employs spread spectrum techniques to differentiate the signal from the noise. This is essential since at the antenna the GPS signal is typically about 20 dB below ambient cosmic noise. "Spread spectrum" means that the frequency or instantaneous phase of the signal being transmitted changes as a function of time. Using spread spectrum signal processing techniques, the receiver can track the spread spectrum signal coming from the satellite by estimating a duplicate image of the signal. A precise match of the satellite's spread spectrum signal produces a potential signal processing gain of up to 53 decibels.

Each satellite generates two spread spectrum signals centered around separate frequencies. The L1 channel is centered about 1575.42 MHz, and has course/acquisition-(C/A-) code and precision-(P-) code modulated on it. C/A-code has a 1.023 MHz chipping rate with a band width of about 2 MHz, and P-code has a 10.23 MHz chipping rate with a bandwidth of about 20 MHz. The L2 channel is centered around 1227.6 MHz and only has P-code modulated on it.

For some applications it is desirable to track both L1 and L2. A position can be derived from just the C/A-code or P-code on the L1 band. However, there is ionospheric delay that unpredictably affects the perceived range to the satellite from the receiver. These errors can be corrected by tracking both L1 and L2 and by measuring the difference in the range that is perceived by the receiver on these L-bands. In this manner, the ionospheric errors can be reduced and the navigation solution can be made more accurate by a few meters. In addition, tracking both L bands simultaneously provides more anti-jamming immunity for operation in hostile environments.

The easiest way to track L1 and L2 is with an in-

dependent tracking loop for each channel. In all implementations to date, either a single channel is multiplexed between L1 and L2 to reduce hardware requirements or an additional complete hardware channel is provided. This either compromises performance and increases software complexity or increases hardware. In either case, this capability adds significant cost to the receiver.

For some operational scenarios, it may also be desirable to be able to switch between having two independent tracking loops and having one tracking loop with a phase delta between L1 and L2. Two independent loops will be used in hostile environments where there is a good possibility of losing either L1 or L2.

As an example of the problem, consider the situation of navigating above 80° latitude north. Above 80° latitude, the Northern Lights and sun spot activity in the north pole make the ionosphere so active that there is the need for frequent L1 and L2 calculations to maintain GPS system accuracy. Using present systems, performing these frequent L1 and L2 calculations makes it is necessary to add additional hardware channels to the receiver. This increases space and cost for each receiver, and increases processor throughput and software complexity. Computer resources to support the increased number of hardware channels forces the user to make some performance compromises. If a system existed that can track L1 and L2 without the penalty of additional hardware, increased computer throughput and increased software complexity it would have value for the GPS user community.

In known systems, it has been necessary to use two channels to track both L1 and L2. The same P-code information is transmitted on the L1 and L2 bands. However, the receiver sees a phase shift between the two signals because of ionospheric delay. The amount of delay is a function of the level of the ionospheric influence. Therefore, if it were possible to use the fact that this information is related, then it may not be necessary to use two wholly independent channels for tracking L1 and L2.

Accordingly, a need exists in the art for a system and method of tracking both L1 and L2 in a GPS receiver without resorting to two distinct hardware channel receivers or time sharing a single channel.

A further need exists in the art for such a receiver designed in a way so as to minimize power consumption and size.

A further need exists in the art for method and system of providing a GPS receiver which allows for both single and double looped processing of L1 and L2 interchangeably. This allows for selecting between the high jamming immunity of tracking L1 and L2 independently or the processor throughput savings of tracking L1 and L2 together.

## SUMMARY OF THE INVENTION

Accordingly, the present invention provides inventive subject matter which overcomes the problems associated with ionospheric delay in Global Positioning System (GPS) receivers. In particular, the present invention provides a single enhanced precision code (P-code) channel for use in a GPS receiver that can simultaneously track L1 and L2 from a single satellite.

The enhanced P-code channel includes a single P-code clock generator for generating two code clock signals (L1 and L2) with the same frequency but a different phase. A P-code generator uses one of the P-code clocks to generate a continuous P-code data stream. Circuitry then stores a plurality of the most recently generated P-code chips. A counter and multiplexer circuit is then used to maintain a constant P-code stream (which may be delayed from the output of the P-code generator) by using one of the P-code clocks. In addition, carrier generation and mixing circuitry, code delay shift registers and mixing circuitry, and multiple pre-detection accumulators exist to allow for the simultaneous tracking of L1 and L2 signals.

A technical advantage of the present system is that, by enhancing a single P-code channel, it is possible to obtain the benefit of independent L1 and L2 tracking loops within a GPS system without the penalty of having two independent hardware channels for this purpose.

Another technical advantage of the present invention is that it is possible to gain the benefit of tracking L2 in addition to L1 to reduce error introduced by ionospheric delay, without the additional processor throughput requirements of tracking L2 independently.

Yet another technical advantage of the present invention is that it permits making continual L1 and L2 calculations without the need for additional computing and support equipment.

## BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be acquired by referring to the detailed description and claims when considered in connection with the accompanying drawings in which like reference numerals indicate like features wherein:

FIGURE 1 is a block diagram of a GPS receiver that may use the enhanced L1/L2 channel of the present invention;

FIGURE 2 is a block diagram of a typical C/A- and P-code channel for use in a GPS receiver for receiving L1 and L2.

FIGURE 3 is a block diagram of a preferred embodiment of the enhanced P-code channel for tracking L1 and L2 for GPS applications;

FIGURE 4 is a block diagram representing the P-code clock generator according to a preferred

embodiment of the present invention;

FIGURE 5 provides a comparison chart between a typical and enhanced P-code channel for tracking L1 and L2 of the present invention.

Figure 6 shows a block diagram of PCOAC 1010. Unused functions can be turned off allowing for a high level of power conservation in applications where power usage and/or heat dissipation is an important consideration.

Figure 7 is a block diagram of the top level modules which electrically make up channel A(11) of PCOAC 10: Base Band Module 1130 generates several global clocks for system synchronization;

## DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment of the present invention is best understood by referring to the FIGURES wherein like numbers are used for like corresponding parts of the various components.

To understand the present invention, it is best to understand the environment of the preferred embodiment. For this purpose, FIGURE 1 provides a simple block diagram of a Global Positioning System (GPS) navigation receiver. The system of FIGURE 1 is described in more detail in U.S. Patent Application Serial No. (TI Docket No. TI-15358) to John P. Volpi et al and assigned to Texas Instruments Incorporated entitled "System and Method for Digital Navigation Satellite Receiver" and U.S. Patent Application Serial No. (TI Docket No. TI-15357) to Leonard LaPadula III, et al, also assigned to Texas Instruments Incorporated, entitled "Method and System for Multi-Channel and Search Global Position System Signal Processor" both filed on February 28, 1991. U.S. Patent Application Serial Nos. and

are hereby expressly incorporated by reference in their entirety.

FIGURE 1 is a simple block diagram of the whole receiver. A single RF path amplifies and down-converts the L1 or L2 signal to an intermediate frequency (IF). The receiver performs analog-to-digital conversion before any GPS signal processing takes place. After the signal is digitized, the signal is processed in three signal processing chips (SPC). The SPCs perform all the GPS hardware signal processing.

Referring more particularly to FIGURE 1, there is shown receiver 10 which utilizes antenna 12 feeding into preamp assembly 14. Antenna preamp assembly 14 feeds into L1/L2 frequency selector 16 which sends signals to L-band down conversion 18. These components all operate under the control of reference oscillator 20 and frequency synthesizer 22. Reference oscillator 20 and frequency synthesizer 22 provide oscillation for L-band down conversion 18. Output from L-band down conversion 18 is a second IF that goes into an analog-to-digital converter (A/D)

with automatic gain control (AGC) circuit 24. The output of this A/D circuit is then channelized to code and carrier wipe off in circuits 26, 28 and 30. This is where the remote signal transmitted by the GPS satellite is compared and matched with the receiver's estimate of the remote signal.

The outputs of signal processing circuits, 26, 28 and 30 are shown as signals 32 into processor computer 34. Processor computer 34 provides signals 36 to signal processing circuit 26, 28 and 30 to direct the circuits to change their code and carrier estimates, as well as for general control of the circuits.

Each signal processing circuit 26, 28 and 30, uniquely and completely generates carrier estimates, code estimates, base band pre-detection estimates and contains all the correlators for signal processing as well as provides autonomous signal search capability for two satellites. Each channel also has the capability to simultaneously track both the C/A-code and P-code, wherever used herein the term P-code shall include P(Y)-code.

FIGURE 2 shows how a typical method to perform pre-detection integration in single C/A- and P-code channel 20 can only track L1 C/A- and P-code or L2 P-code. Carrier generator 36 generates a complex estimate of the incoming GPS carrier. Carrier mixer 38 wipes off the incoming carrier. P-code clock generator 40 and P-code generator 42 generate an estimate of P-code and C/A- code clock generator 44 and C/A-code generator 46 generate an estimate of the C/A-code. P-code delay shift register 48 and C/A-code delay shift register 50 generate a plurality of P-code and C/A-code phases 1/2-chip apart, respectively. Finally, code is wiped off in P-code mixers 52 and C/A-code mixers 54. Pre-detection integration is then performed using an integrate circuit 56.

Six correlators are shown so the P-code and C/A-code can be track simultaneously (three for P-code and three for C/A-code). In addition, it is possible to dedicate all six correlators to C/A-code using correlator switches 58 for search modes of operation. This is done so that C/A-code can be found more quickly in typical search operations.

For some applications of GPS, it is desirable to be able to track L1 and L2 simultaneously. Hardware aside, the easiest way to do this is with an independent tracking loop for L1 and L2. By enhancing the previously described channel 37, it is possible to get the benefit of independent L1 and L2 tracking without the penalty of having two independent channels. For some operational scenarios, it also may be desirable to be able to switch between having two independent tracking loops and having one tracking loop with a phase delta between L1 and L2. Two independent loops would be used in hostile environments where there is a good possibility of losing either L1 or L2. One tracking loop may be desirable for less processor

throughout when there is no threat of losing the main L-band. Within a P-code receiver such as that of FIGURE 1, the present invention allows this operational flexibility. For these purposes, FIGURE 3 describes an enhanced single P-code L1/L2 channel that may be used to enhance the capability of signal processing circuits 26, 28 and 30.

FIGURE 3 shows an enhanced L1/L2 channel 60 according to the present invention. The modified P-code clock generator 62 generates two P-code clocks with same frequency and independent phase, one for L1 and one for L2. The modified P-code clock generator 62 also detects which of these clock lead. The leading clock is used to clock P-code generator 64. Each new P-code chip is stored in the next location of the P-code circular buffer 302. P-code clock generator 62 is used to increment the L1 and L2 P-code chip counters 68 and 70, respectively. Whenever the L1 P-code chip counter, 68, is incremented, 16-to-1 MUX 70 passes the next P-code chip stored in the P-code circular buffer 66 to the L1 P-code delay shift register 76. The L2 P-code chip counter 72 and 16-to-1 MUX 74 are implemented and work in exactly the same manner as the L1 P-code chip counter 68 and 16-to-1 MUX, 70. Thus, from one P-code generator 64 two P-code outputs, one for L1 and one for L2, go to code delay shift registers, 76 and 78, respectively. This represents a considerable savings in circuitry because P-code generator 64 comprises numerous gates and additionally requires significant computer processing capability to support its operation. Although the preferred embodiment requires a separate carrier generator for each signal frequency, carrier generators for L1 and L2 are easy to build and do not consume nearly as much power as would a second complete channel.

The enhanced L1/L2 channel 60 of FIGURE 3 provides maximum operational flexibility with minimal additional circuitry. Circuits which are not changed from the previously described typical C/A- and P-code channel include the P-code generator 64, C/A-code clock generator 44, and C/A-code generator 46. The carrier generators, 80 and 82, and carrier mixers, 84 and 86 are the same as the previously shown carrier generator 36 and carrier mixer 38, except that L1 carrier generator 80 is always configured to generate an L1 carrier and the L2 carrier generator 82 is always configured to generate an L2 carrier. Also, the code delay shift registers, 76, 78 and 88, code mixers, 90, 92 and 94, the pre-detection integration circuitry 96, and correlator switches 98 and 100 are implemented and function such as the code delay shift registers 48 and 50, code mixers, 52 and 54, the pre-detection integration circuitry 56 and the correlator switches 58 shown in the typical C/A- and P-code channel 37 of FIGURE 2. The only difference being that there is an extra set of P-code delay shift registers 78, P-code mixers 92 and correlator switches 100 and that the

pre-detection integration circuitry 332 supports three additional correlators. This is done to accommodate the extra three correlators required to track L2 P-code.

Unique to the enhanced channel is a modified P-code clock generator 62, a P-code circular buffer 66, two P-code chip counters, 68 and 72, and two 16-to-1 multiplexers (MUX), 70 and 74.

FIGURE 4 shows a high level block diagram of the modified P-code clock generator 62. This circuit is a unique modification of the low-powered digital oscillator detailed in co-pending application entitled "Method and Systems for a Multi-Channel Global Position System Signal Processor". Circuitry to determine which clock leads is not shown. One approach to determine the leading clock is to extend the P-code chip counters 68 and 74 an extra two bits and compare the counter values to see which clock leads.

The circuit operation of the modified P-code clock generator 62, is basically the same as the code clock generator described in the previously mentioned co-pending U.S. Patent Applications. The modification is that there are two separate 16-bit P-code clock phase words 112 and 114, one for determining the phase of the L1 P-code clock and the other for determining the phase of the L2 P-code clock. Since initial P-code clock phase only affects the 13 most significant bits of the 32-bit P-code clock generator adder/accumulator, the 19 least significant bits of the adder/accumulator 122 are common to both the L1 and the L2 P-code clock. The frequency word 116 is also common to both the L1 and L2 P-code clock. Along with the two separate P-code clock phase words, 112 and 114 are two 13-bit adder/accumulators 118 and 120 one for L1 P-code clock and one for L2 P-code clock, which together with the 19-bit adder/accumulator 122 make up two separate 32-bit adder/accumulators capable of generating carriers to the two state machines 124 and 126 with the same frequency but different phase. The state machine and carry delay circuits 124 and 126 are exactly the same as described in the previously mentioned co-pending U.S. Patent Applications.

FIGURE 5 shows the estimated difference between a typical single L-band channel and the enhanced L1/L2 channel of the present invention. An enhanced channel requires only 42% additional circuitry over a normal channel and provides the performance benefit and software reduction of two completely independent channels for tracking L1 and L2 simultaneously.

The cost of the enhanced channel is considerably less than the 42% when overhead circuitry such as channel timing and control, processor interface and search specific circuits are included in the gate count estimates. Also note that for this specific example, that the enhanced channel has three additional correlators. This provides approximately a 50% improvement in search speed. As a result of the enhanced P-

code channel of the present invention, there is provided an apparatus and method for significantly increasing GPS system receiver channel flexibility without a significant increase in circuitry or software complexity.

Although this description describes the invention with reference to the above specific embodiments, the claims, and not this description, limit the scope of the invention. Various modifications or the disclosed embodiment, as well as alternative embodiments of the invention, will become apparent to persons skilled in the art upon reference to the above description. Therefore, the appended claims will cover such modification that follow up in the true scope of the invention.

Aspects of the present invention will be further appreciated from the following:

The P-Code Channel on-a-chip (PCOAC) to be described is a dual channel GPS signal processor integrated circuit. A 95-pin ceramic pin-grid-array (PGA) contains the 348,300 transistor CMOS gate array. Major features include: two independent GPS channels; a search processor for improved acquisition time; an embedded Y-code generator; system synchronization control; and a 16-bit processor interface.

Figure 16 shows a block diagram of PCOAC 1010. Unused functions can be turned off allowing for a high level of power conservation in applications where power usage and/or heat dissipation is an important consideration.

Each channel of circuit 1010 is a dedicated signal processing circuit which de-modulates the code and carrier of a GPS signal and performs pre-detection integration. Each channel contains a code clock generator 1103 (1104), a P and C/A-code generator 1105 (1106), an L1/L2 carrier generator 1109 (1110), eight correlators 1111, 1113, 1115, 1117 (1112, 1114, 1116, 1118) and a noise meter 1119 (1120). Each of the eight correlators can be selected to operate with C/A-code or P-Code. A Y-code generator 1108 common to both channels provides independent Y-code for both channels.

Search processor 1123 and discrete fourier transform (DFT) function 1124 improve signal acquisition capability. The DFT separates the sample integration data into seven frequency bins. Search processor 1123 interpolates between these seven frequency bins to obtain six additional frequency bins, producing a total of thirteen frequency bins per correlator. The search processor implements a Tong detection algorithm on all eight correlators for each of the thirteen frequency bins resulting in the simultaneous search of 1104 search bins per channel.

PCOAC 1010 supports three frequency plans, 57.7920 MHz, 40.9216 MHz and 40.9200 MHz operation. Several programmable clocks/interrupts 1130 are provided to synchronize the host processor to

PCOAC operation. Various interrupt schemes are designed to allow trade-offs to be made between system performance, processor throughput requirements and the complexity of the software.

A standard 16-bit processor interface 1131 is utilized. In order to minimize read/write overhead to the PCOAC, integration samples are buffered 1121 (1122) and the memory map is designed so that block moves are all that is required for channel updates during normal tracking operations.

Figure 7 is a block diagram of the top level modules which electrically make up channel A(11) of PCOAC 10: Base Band Module 1130 generates several global clocks for system synchronization;

Channel Timing Module 1101 generates all clocks and synchronization pulses specific to a single channel;

Code Generator Module 21 includes a programmable code clock generator, P-code and C/A-code generators/setters, and P-code and C/A-code state advance and retard for search;

Y-Code Generator Module 1108 converts the P-code into Y-code for both channels simultaneously even during code state advances;

Front-End Correlator Module 1201 provides L1 or L2 carrier generation, a carrier mixer, a P-code and C/A-code delay shift register (to generate eight code phases), code mixers, data wipe-off, and noise meter signal selection;

Intermediate Correlator Module 1202 performs the first stage of sample integration for eight complex correlators and a noise meter;

Black-End Correlator Module 1203 performs the final stage of sample integration, and also performs noise measurement for aiding in search and tracking (one per channel);

IRAM 1204 and Q RAM 1205 are two 64 x 16-bit 3-port RAMs per channel for sample integration buffering or to hold intermediate values for DFT calculations;

Discrete Fourier Transform (DFT) Module 1124 converts integration samples from all correlators of both channels into seven frequency bins of sample data for search operations;

Search Processor Module 1206 interpolates six additional frequency bins from those provided by the DFT module, performs Tong detection on all thirteen frequency bins of data and retards the code state until a signal is found;

Search Processor RAM 1207 is a 64 x 16-bit 3-port RAM used by the search processor as a holding register for active Tong counts during search or noise measurement buffering during tracking;

Processor Interface Module 1131 provides address decode to generate internal read and write strobes, integration sample buffering control, a programmable ring oscillator for test and other miscellaneous functions.

Digital signal processing circuitry as exemplified herein may be implemented by means of a single integrated circuit.

## Claims

1. An enhanced P-code channel for use in a GPS receiver, said channel being adapted for simultaneously tracking L1 and L2 and comprising:
  - a P-code clock generator for generating two code clocks, the first clocks associated with L1 and the second of said code clocks associated with L2, said code clocks having the same frequency but different phase from one another;
  - circuitry for generating a plurality of P-code chips and storing a plurality of the most recently generated of said P-code chips;
  - a first circuit for selecting and update P-code chips from said stored plurality of P-code chips said selected and updated chips being in phase with said L-1 code clock;
  - a second circuit for selecting and updating P-code chips from said stored plurality of P-code chips said selected and updated chips being in phase with said L-2 code clock.
2. A multi-channel GPS signal processor for use in a GPS receiver, said processor comprising:
  - digital signal processing circuitry on a single integrated circuit for acquiring and tracking valid P-code signals from at least one satellite of said GPS system; and
  - an enhanced P-code channel as claimed in claim 1.
3. A receiver for determining geographical position, velocity, and time from analog signal information received from a plurality of navigational satellites, said signal information having data shifts dependent upon distance and frequency shifts dependent upon the relevant velocity between the satellite's transmission position and the geographical position of said receiver, wherein said analog signal is significantly weaker than ambient atmospheric noise, said receiver comprising:
  - a digital signal processing circuit for acquiring said signal in the presence of said noise, for estimating the current position and for correcting said estimate based upon data exchanged between said digital signal processing circuit and said processor;
  - an enhanced P-code channel associated within said digital processing circuit for use in said receiver, said channel capable of simultaneously tracking L1 and L2 and comprising:
    - a single P-code clock generator for generating two code clocks, a first of said code clocks asso-

- ciated with L1 and a second of said code clocks associated with L2, said code clocks having the same frequency but different phase from each other;
- circuitry for generating a plurality of P-code chips and storing a plurality of said P-code chips, said P-code chips being those most recently generated by said digital signal processing circuit;
- a first circuit for selecting and updating P-code chips from said plurality of chips, said chips being in phase with said L1 code clock; and
- a second circuit for selecting and updating P-code chips from said stored plurality of chips, said chips being in phase with said L2 code clock.
4. The apparatus of any of Claims 1-3, further comprising a P-code circular buffer within said generating and storing circuitry for generating two phases of P-code for tracking L1 and L2.
  5. The apparatus of Claim 4, wherein said channel is associated to independently track L1 or L2.
  6. The apparatus of any of Claims 1-3, further comprising circuitry for simultaneously generating C/A-code for L1, P-code for L1, and P-code for L2.
  7. The apparatus of Claim 6, further comprising circuitry for vector summing said C/A-code for L1, P-code for L1, and P-code for L2, thereby increasing sensitivity of said channel.
  8. The apparatus of any of Claim 1-3, further comprising circuitry for continuous ionospheric correction within said channel.
  9. A method for simultaneously tracking L1 and L2 in a single P-code channel for use in the GPS receiver, said method comprising the steps of:
    - generating two code clocks using a single P-code clock generator, the first of said code clocks being associated with L1 and the second of said code clocks being associated with L2, said code clocks further having the same frequency but different phases;
    - generating a plurality of P-code chips;
    - storing a plurality of the most recently generated of said P-code chips;
    - selecting and updating P-code chip addresses from said stored plurality of P-code chips in phase with said L1 code clock; and
    - selecting and updating P-code chips from said stored plurality of chips in phase with said L2 code clock.
  10. The method of Claim 9, further comprising the step of tracking L1 in said channel for assisting L2 tracking.
  11. The method of Claim 9, further comprising the step of tracking L2 in said channel to a tracking of L1.
  12. A method for determining geographical position, velocity, and time from analog signal information received from a plurality of navigational satellites, said signal information having data shifts depending upon distance and frequency shifts depended upon the relative velocity between the satellite's transmission position and the geographical position of said receiver, wherein said analog signal is significantly weaker than ambient atmospheric noise, said method comprising the steps of:
    - acquiring said signal in the presence of said noise, estimating the current position, and correcting said estimate; and
    - simultaneously tracking L1 and L2 in a single enhanced P-code channel said tracking step comprising the steps of:
      - generating two code clocks using a single P-code clock generator the first of said code clocks being associated with L1 and the second of said code clocks associated with L2, said code clocks further having the same frequency but different phases;
      - generating a plurality of P-code chips;
      - storing a plurality of the most recently generated of said P-code chips;
      - selecting and updating P-code chip addresses from said stored plurality of P-code chips in phase with said L1 code clock; and
      - selecting and updating P-code chips from said stored plurality of chips in phase with said L2 code clock.
  13. The method of Claim 12, further comprising the step of generating two phases of P-code for tracking L1 and L2 separately.
  14. The method of either of Claims 9 or 12, further comprising the step of independently tracking L1 or L2.
  15. The method of either Claims 9 or 12, further comprising the step of simultaneously generating C/A-code for L1, P-code for L1, and P-code within said single enhanced channel.
  16. The method of Claim 15, further comprising the step of vector summing said C/A-code for L1, P-code for L1 and P-code for L2.
  17. The method of either of Claims 9 or 12, further

comprising the step of continuously performing  
ionospheric correction within said channel.

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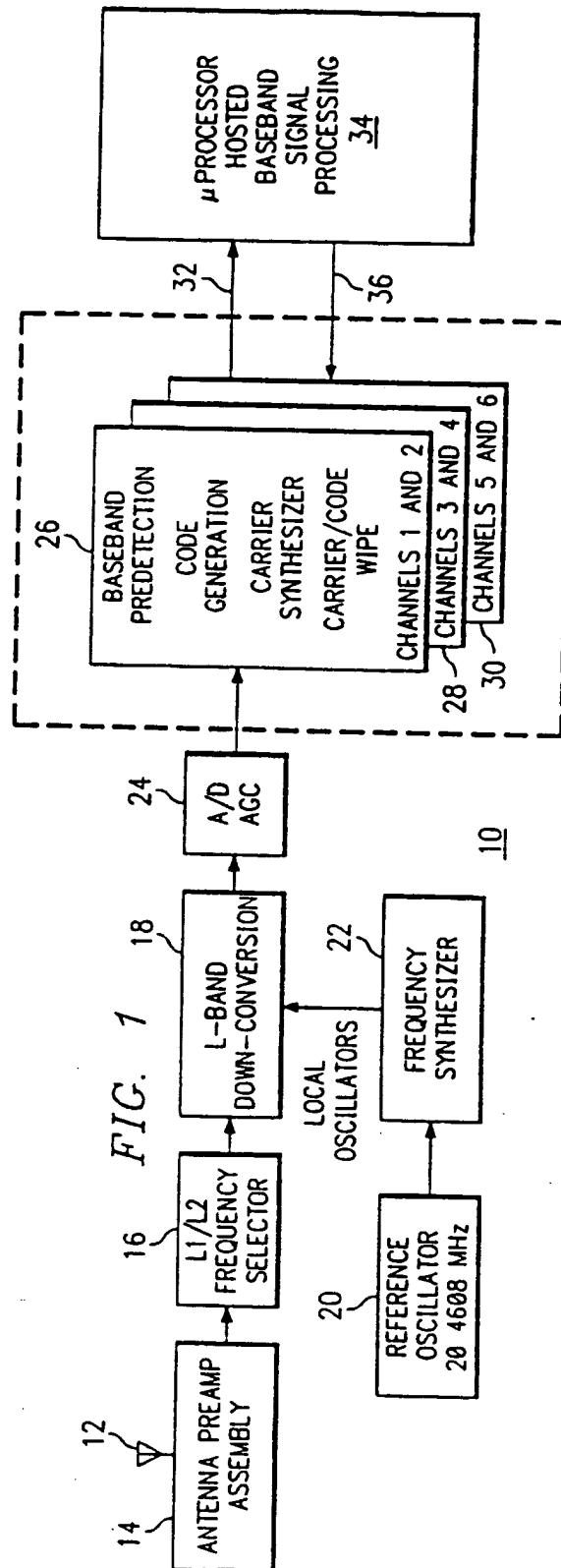
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SEE FIGS. 2 & 3

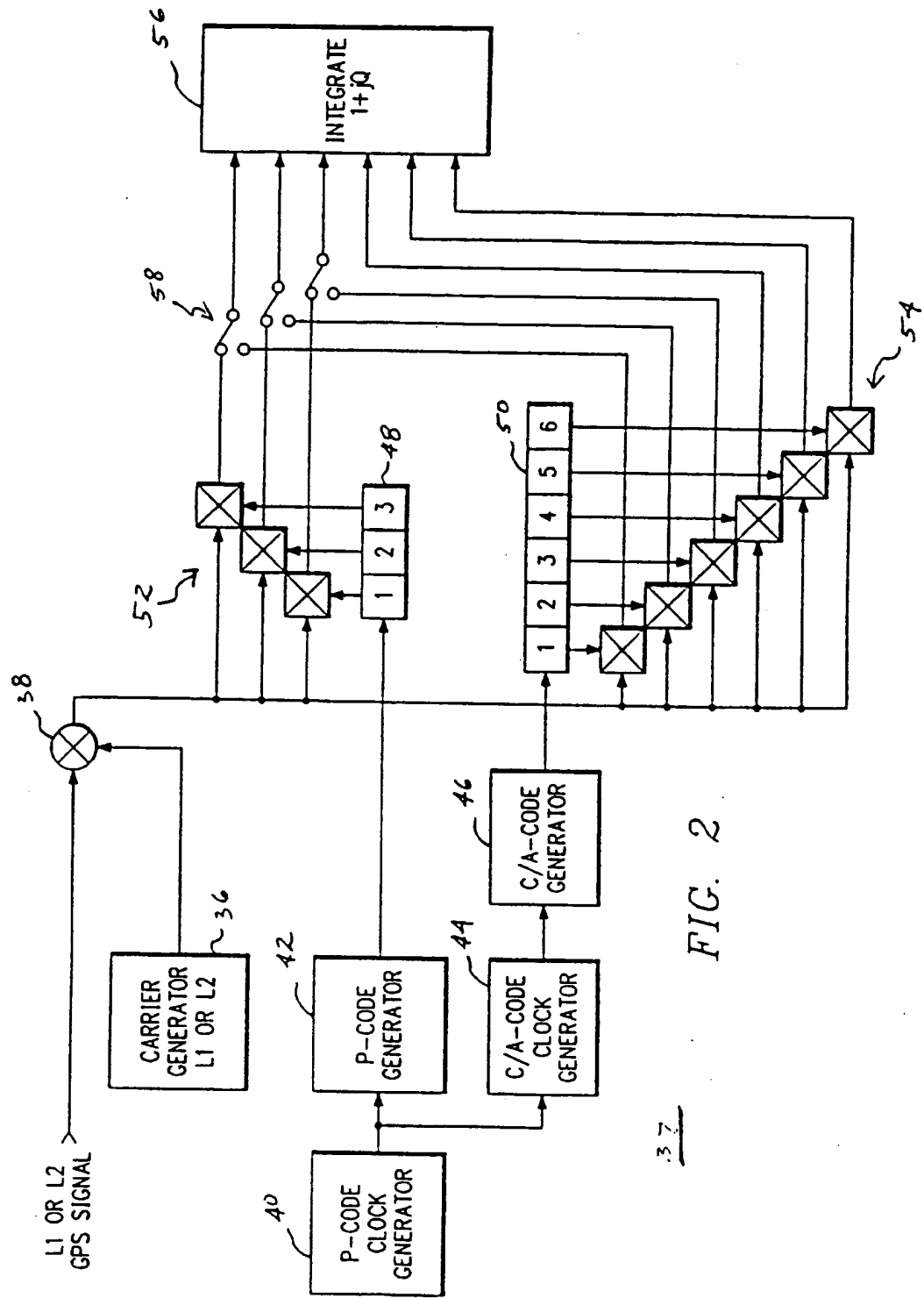


FIG. 2



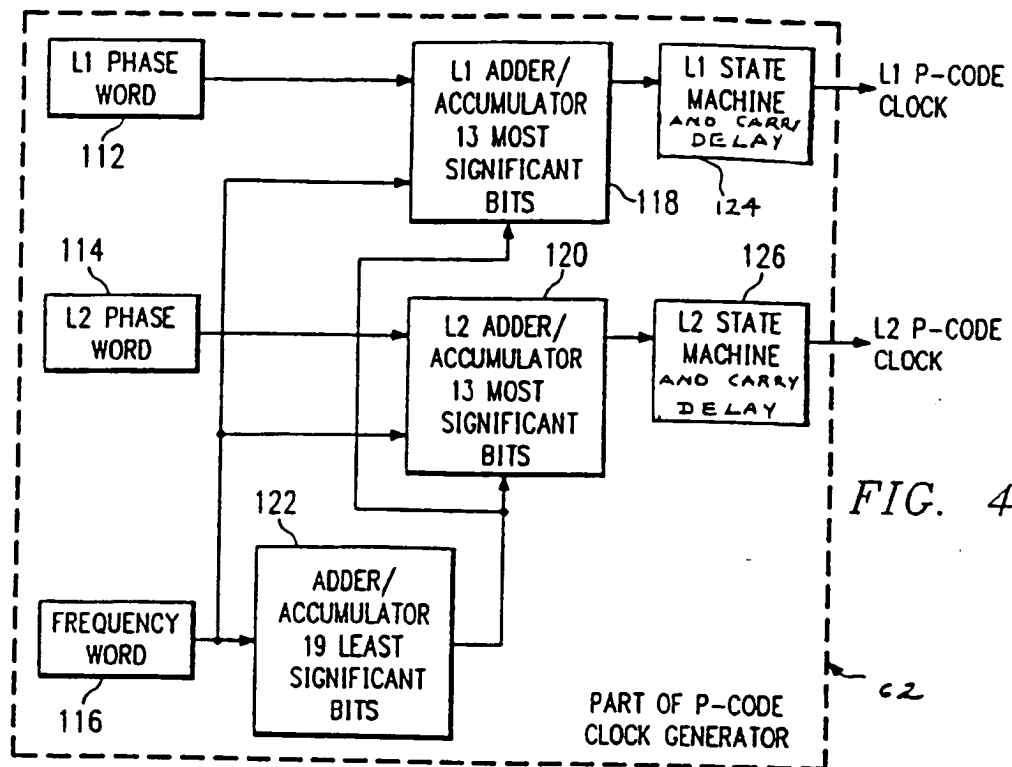
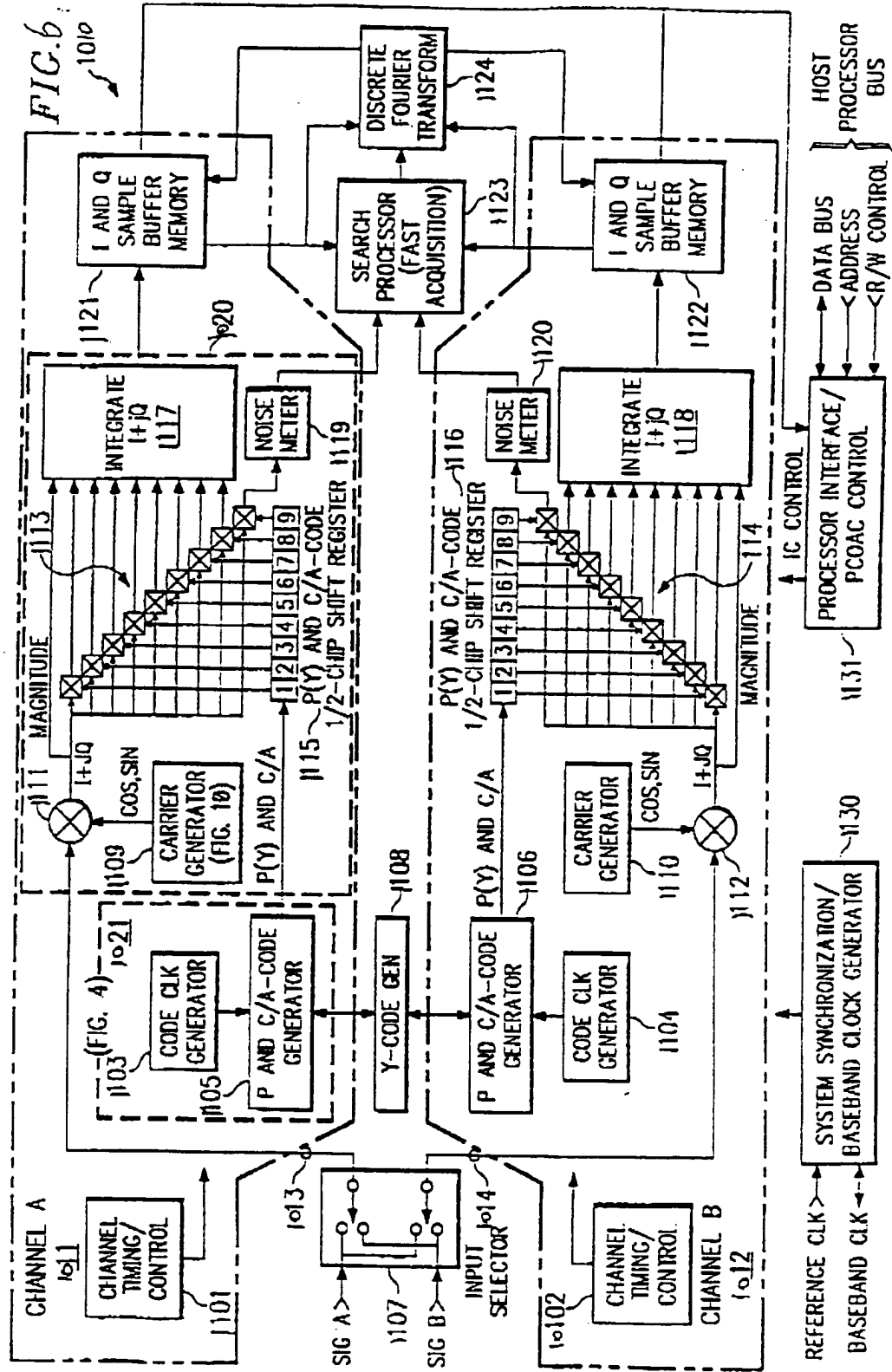


FIG. 5 GATE COUNT OF PRIOR ART CHANNEL VERSUS ENHANCED L1/L2 CHANNEL

FUNCTION	TYPICAL		ENHANCED	
	QTY	GATES	QTY	GATES
CARRIER GENERATOR 36, 80, 82	1	1244	2	2488
CARRIER MIXER 38, 84, 86	1	126	2	252
P-CODE CLOCK GEN. 40, 62	1	1246	1.5	1869
P-CODE GENERATOR 42, 64	1	3000	1	3000
CIRCULAR BUFFER 66	0	0	1	150
COUNTER 68, 72	0	0	2	60
16:1 MULTIPLEXER 70, 74	0	0	2	66
P-CODE DELAY SHIFT REG. 48, 76, 78	1	25	2	50
P-CODE MIXERS 52, 90, 92	3	9	6	18
C/A-CODE CLOCK GEN. 44	1	50	1	50
C/A-CODE GEN. 46	1	500	1	500
C/A-CODE DELAY SHIFT REG. 50, 88	1	50	1	75
C/A-CODE MIXERS 54, 94	6	18	9	27
CORRELATOR SWITCH 58, 98, 100	3	9	6	18
INTEGRATORS 56, 96	6	4100	9	6150
TOTAL	10,377		14,773	



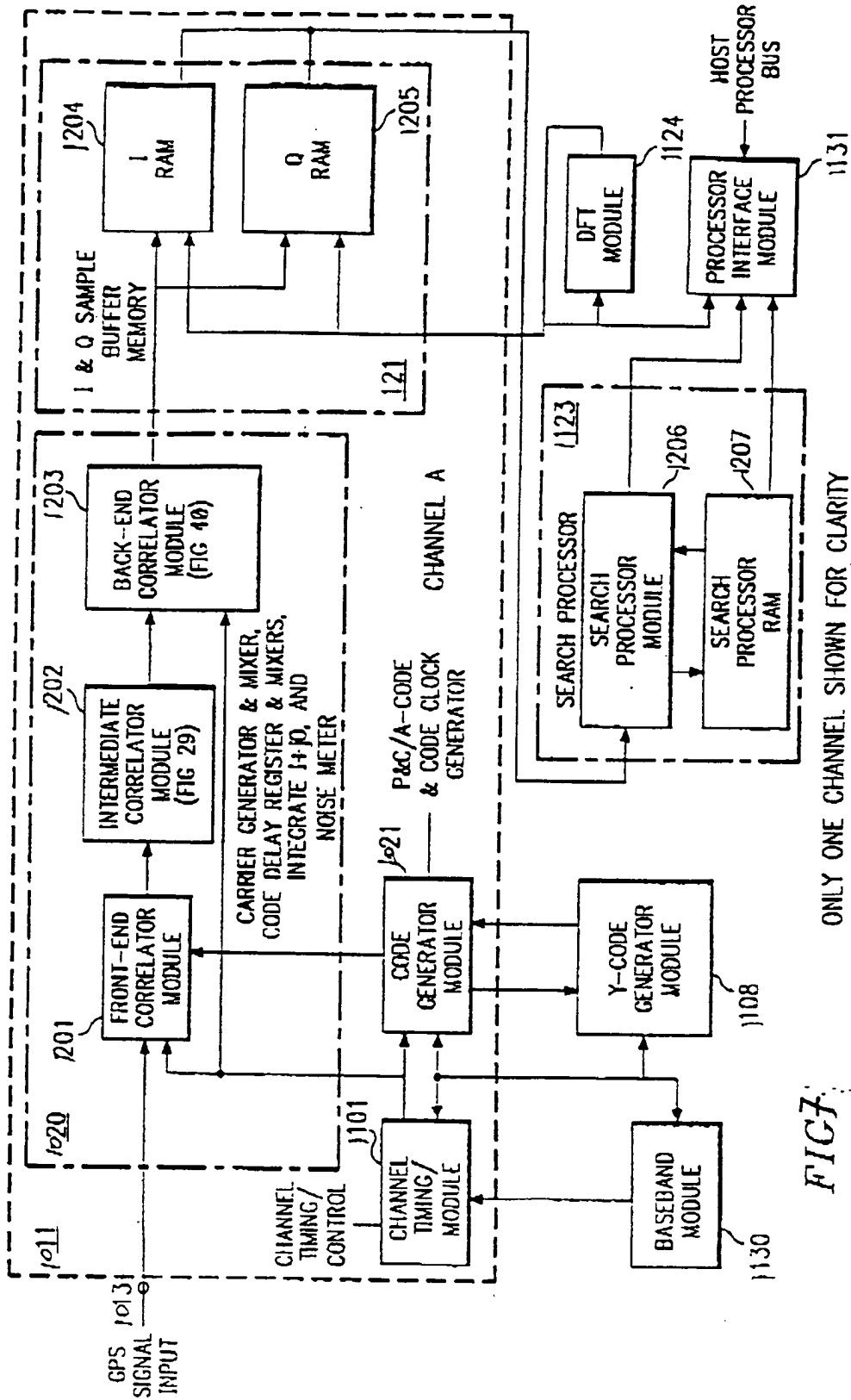


FIG. 1

ONLY ONE CHANNEL SHOWN FOR CLARITY



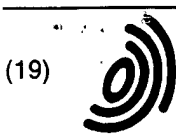
European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number

DOCUMENTS CONSIDERED TO BE RELEVANT			EP 92302791.6
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	<u>US - A - 4 035 663</u> (ROCKWELL)	1-3, 9, 12	G 01 S 5/08 G 01 S 11/08
A	* Abstract; claims *	4-8, 10, 11, 13-17	
Y	<u>US - A - 4 613 977</u> (STC)	1-3, 9, 12	
A	* Abstract; claims *	4-8, 10, 11, 13-17	
A	<u>US - A - 4 189 622</u> (NCR)	1-17	
	* Abstract; claims *		
A	<u>US - A - 4 468 793</u> (TI)	1-17	
	* Abstract; claims *		
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G 01 S 5/00 G 01 S 11/00 H 03 K 19/00 H 04 B 1/00 H 04 L 7/00
The present search report has been drawn up for all claims			
Place of search <b>VIENNA</b>		Date of completion of the search <b>25-05-1992</b>	Examiner <b>BLASL</b>
<b>CATEGORY OF CITED DOCUMENTS</b> X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		I : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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(54) **Enhanced L1/L2 code channel for global positioning system receivers**

L1/L2-Code-Frequenzband für Global-Positioning-System-Receiver

Bande de fréquence à code L1/L2 pour récepteur de système positionnement global

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(73) Proprietor: **TEXAS INSTRUMENTS  
INCORPORATED  
Dallas Texas 75265 (US)**

(72) Inventors:  
• **Lapadula, Leonard, III  
Garland, TX 75050 (US)**

• **Scott, Hugh L.  
Colorado Spring, CO 80919 (US)**  
• **Volpi, John P.  
Carrollton, TX 75007 (US)**

(74) Representative: **Nettleton, John Victor et al  
Abel & Imray  
Northumberland House  
303-306 High Holborn  
London, WC1V 7LH (GB)**

(56) References cited:  
**US-A- 4 035 663 US-A- 4 189 622**  
**US-A- 4 468 793 US-A- 4 613 977**

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**EP 0 511 741 B1**



## Description

### TECHNICAL FIELD OF THE INVENTION

This invention relates to Global Positioning System (GPS) receivers and more particularly a method for enhancing a single receiver channel for processing a plurality of L-band signals.

### BACKGROUND OF THE INVENTION

The NAVSTAR Global Positioning System (GPS) is used to determine exact geographic position (i.e. latitude, longitude, and height above the earth) as well as the exact velocity and time of stationary or moving objects. The navigation receiver calculates position, and time by determining distance to a series of satellites. The navigation receiver calculates velocity by determining doppler frequency shift of the satellite signals.

The NAVSTAR GPS receiver must receive signals generated from the satellite about 11,000 miles away. Each GPS satellite transmits a 6-watt signal. The satellite and receiver, therefore, employs spread spectrum techniques to differentiate the signal from the noise. This is essential since at the antenna the GPS signal is typically about 20 dB below ambient cosmic noise. "Spread spectrum" means that the frequency or instantaneous phase of the signal being transmitted changes as a function of time. Using spread spectrum signal processing techniques, the receiver can track the spread spectrum signal coming from the satellite by estimating a duplicate image of the signal. A precise match of the satellite's spread spectrum signal produces a potential signal processing gain of up to 53 decibels.

Each satellite generates two spread spectrum signals centered around separate frequencies. The L1 channel is centered about 1575.42 MHz, and has course/acquisition-(C/A-) code and precision-(P-) code modulated on it. C/A-code has a 1.023 MHz chipping rate with a band width of about 2 MHz, and P-code has a 10.23 MHz chipping rate with a bandwidth of about 20 MHz. The L2 channel is centered around 1227.6 MHz and only has P-code modulated on it.

For some applications it is desirable to track both L1 and L2. A position can be derived from just the C/A- or P-code on the L1 band. However, there is ionospheric delay that unpredictably affects the perceived range to the satellite from the receiver. These errors can be corrected by tracking both L1 and L2 and by measuring the difference in the range that is perceived by the receiver on these L-bands. In this manner, the ionospheric errors can be reduced and the navigation solution can be made more accurate by a few meters. In addition, tracking both L bands simultaneously provides more anti-jamming immunity for operation in hostile environments.

The easiest way to track L1 and L2 is with an independent tracking loop for each channel. In all implementations to date, either a single channel is multiplexed be-

tween L1 and L2 to reduce hardware requirements or an additional complete hardware channel is provided. This either compromises performance and increases software complexity or increases hardware. In either case, this capability adds significant cost to the receiver.

For some operational scenarios, it may also be desirable to be able to switch between having two independent tracking loops and having one tracking loop with a phase delta between L1 and L2. Two independent loops will be used in hostile environments where there is a good possibility of losing either L1 or L2.

As an example of the problem, consider the situation of navigating above 80° latitude north. Above 80° latitude, the Northern Lights and sun spot activity in the north pole make the ionosphere so active that there is the need for frequent L1 and L2 calculations to maintain GPS system accuracy. Using present systems, performing these frequent L1 and L2 calculations makes it is necessary to add additional hardware channels to the receiver. This increases space and cost for each receiver, and increases processor throughput and software complexity. Computer resources to support the increased number of hardware channels forces the user to make some performance compromises. If a system existed that can track L1 and L2 without the penalty of additional hardware, increased computer throughput and increased software complexity it would have value for the GPS user community.

In known systems, it has been necessary to use two channels to track both L1 and L2. The same P-code information is transmitted on the L1 and L2 bands. However, the receiver sees a phase shift between the two signals because of ionospheric influence. The amount of delay is a function of the level of the ionospheric influence. Therefore, if it were possible to use the fact that this information is related, then it may not be necessary to use two wholly independent channels for tracking L1 and L2.

Accordingly, a need exists in the art for a system and method of tracking both L1 and L2 in a GPS receiver without resorting to two distinct hardware channel receivers or time sharing a single channel.

A further need exists in the art for such a receiver designed in a way so as to minimise power consumption and size.

A multi-channel GPS digital signal processor is disclosed in published European application No. 501828 A1. Each channel contains circuitry to process high frequency (L1) band signals and low frequency (L2) band signals of either P-code or C/A-code. The signal processor includes a search processor for fast signal acquisition but does not address problems of power consumption and size.

A further need exists in the art for a method and system of providing a GPS receiver which allows for both single and double looped processing of L1 and L2 interchangeably. This allows for selection between the high jamming immunity of tracking L1 and L2 independ-

ently or the processor throughput savings of tracking L1 and L2 together.

A GPS receiver is disclosed in published European Application No. 501,829 A1 which converts analogue signals to digital signals prior to performing signal acquisition. The receiver includes an A/D converter using full-null-zone processing to increase the anti-jamming capability, but does not address the problem of interchangeably operating single and double looped processing.

The present invention provides apparatus as defined in each of the appended claims 1, 2 and 3 and a method as claimed in claim 10.

A technical advantage of the present system is that, by enhancing a single P-code channel, it is possible to obtain the benefit of independent L1 and L2 tracking loops within a GPS system without the penalty of having two independent hardware channels for this purpose.

Another technical advantage of the present invention is that it possible to gain the benefit of tracking L2 in addition to L1 to reduce error introduced by ionospheric delay, without the additional processor throughput requirements of tracking L2 independently.

Yet another technical advantage of the present invention is that it permits making continual L1 and L2 calculations without the need for additional computing and support equipment.

#### BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be acquired by referring to the detailed description and claims when considered in connection with the accompanying drawings in which like reference numerals indicate like features wherein:

FIGURE 1 is a block diagram of a GPS receiver that may use the enhanced L1/L2 channel of the present invention;

FIGURE 2 is a block diagram of a typical C/A- and P-code channel for use in a GPS receiver for receiving L1 and L2.

FIGURE 3 is a block diagram of a preferred embodiment of the enhanced P-code channel for tracking L1 and L2 for GPS applications;

FIGURE 4 is a block diagram representing the P-code clock generator according to a preferred embodiment of the present invention;

FIGURE 5 provides a comparison chart between a typical and enhanced P-code channel for tracking L1 and L2 of the present invention.

Figure 6 shows a block diagram of P-Code Channel on-a-chip (PCOAC) 1010. Unused functions can be turned of allowing for a high level of power conservation in applications where power usage and/or heat dissipation is an important consideration.

Figure 7 is a block diagram of the top level modules which electrically make up channel A(11) of PCOAC

10: Base Band Module 1130 generates several global clocks for system synchronization;

Figures 6 and 7 correspond to Figures 1 and 2 of EP-A-0 501 828.

#### DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment of the present invention is best understood by referring to the FIGURES wherein like numbers are used for like corresponding parts of the various components.

FIGURE 1 is a simple block diagram of a whole receiver according to the prior art. A single RF path amplifies and down-converts the L1 and L2 signal to an intermediate frequency (IF). The receiver performs analogue-to-digital conversion before any GPS signal processing takes place. After the signal is digitised, the signal is processed in three signal processing chips (SPC). The SPCs perform all the GPS hardware signal processing.

Referring more particularly to FIGURE 1, there is shown receiver 10 which utilises antenna 12 feeding into preamp assembly 14. Antenna assembly 14 feeds into L1/L2 frequency selector 16 which sends signals to L-band down conversion 18. These components all operate under the control of reference oscillator 20 and frequency synthesizer 22. Reference oscillator 20 and frequency synthesizer 22 provide oscillation for L-band down conversion 18. Output from L-band down conversion 18 is a second IF that goes into an analog-to-digital converter (A/D) with automatic gain control (AGC) circuit 24. The output of this A/D circuit is then channelized to code and carrier wipe off in circuits 26, 28 and 30. This is where the remote signal transmitted by the GPS satellite is compared and matched with the receiver's estimate of the remote signal.

The outputs of signal processing circuits, 26, 28 and 30 are shown as signals 32 into processor computer 34. Processor computer 34 provides signals 36 to signal processing circuit 26, 28 and 30 to direct the circuits to change their code and carrier estimates, as well as for general control of the circuits.

Each signal processing circuit 26, 28 and 30, uniquely and completely generates carrier estimates, code estimates, base band pre-detection estimates and contains all the correlators for signal processing as well as provides autonomous signal search capability for two satellites. Each channel also has the capability to simultaneously track both the C/A-code and P-code. wherever used herein, the term P-code shall include P (Y)-code.

FIGURE 2 shows how a typical method to perform pre-detection integration in single C/A- and P-code channel 37. This channel 20 can only track L1 C/A- and P-code or L2 P-code. Carrier generator 36 generates a complex estimate of the incoming GPS carrier. Carrier mixer 38 wipes off the incoming carrier. P-code clock

generator 40 and P-code generator 42 generate an estimate of P-code and C/A-code clock generator 44 and C/A-code generator 46 generate an estimate of the C/A-code. P-code delay shift register 48 and C/A-code delay shift register 50 generate a plurality of P-code and C/A-code phases 1/2-chip apart, respectively. Finally, code is wiped off in P-code mixers 52 and C/A-code mixers 54. Pre-detection integration is then performed using an integrate circuit 56.

Six correlators are shown so the P-code and C/A-code can be track simultaneously (three for P-code and three for C/A-code). In addition, it is possible to dedicate all six correlators to C/A-code using correlator switches 58 for search modes of operation. This is done so that C/A-code can be found more quickly in typical search operations.

For some applications of GPS, it is desirable to be able to track L1 and L2 simultaneously. Hardware aside, the easiest way to do this is with an independent tracking loop for L1 and L2. By enhancing the previously described channel 37, it is possible to get the benefit of independent L1 and L2 tracking without the penalty of having two independent channels. For some operational scenarios, it also may be desirable to be able to switch between having two independent tracking loops and having one tracking loop with a phase delta between L1 and L2. Two independent loops would be used in hostile environments where there is a good possibility of losing either L1 or L2. One tracking loop may be desirable for less processor throughput when there is no threat of losing the main L-band. Within a P-code receiver such as that of FIGURE 1, the present invention allows this operational flexibility. For these purposes, FIGURE 3 describes an enhanced single P-code L1/L2 channel that may be used to enhance the capability of signal processing circuits 26, 28 and 30.

FIGURE 3 shows an enhanced L1/L2 channel 60 according to the present invention. The modified P-code clock generator 62 generates two P-code clocks with same frequency and independent phase, one for L1 and one for L2. The modified P-code clock generator 62 also detects which of these clock lead. The leading clock is used to clock P-code generator 64. Each new P-code chip is stored in the next location of the P-code circular buffer 302. P-code clock generator 62 is used to increment the L1 and L2 P-code chip counters 68 and 72, respectively. Whenever the L1 P-code chip counter, 68, is incremented, 16-to-1 MUX 70 passes the next P-code chip stored in the P-code circular buffer 66 to the L1 P-code delay shift register 76. The L2 P-code chip counter 72 and 16-to-1 MUX 74 are implemented and work in exactly the same manner as the L1 P-code chip counter 68 and 16-to-1 MUX, 70. Thus, from one P-code generator 64 two P-code outputs, one for L1 and one for L2, go to code delay shift registers, 76 and 78, respectively. This represents a considerable savings in circuitry because P-code generator 64 comprises numerous gates and additionally requires significant computer process-

ing capability to support its operation. Although the preferred embodiment requires a separate carrier generator for each signal frequency, carrier generators for L1 and L2 are easy to build and do not consume nearly as much power as would a second complete channel.

The enhanced L1/L2 channel 60 of FIGURE 3 provides maximum operational flexibility with minimal additional circuitry. Circuits which are not changed from the previously described typical C/A- and P-code channel include the P-code generator 64, C/A-code clock generator 44, and C/A-code generator 46. The carrier generators, 80 and 82, and carrier mixers, 84 and 86 are the same as the previously shown carrier generator 36 and carrier mixer 38, except that L1 carrier generator 80 is also always configured to generate an L1 carrier and the L2 carrier generator 82 is always configured to generate an L2 carrier. Also, the code delay shift registers, 76, 78 and 88, code mixers, 90, 92 and 94, the pre-detection integration circuitry 96, and correlator switches 98 and 100 are implemented and function such as the code delay shift registers 48 and 50, coder mixers, 52 and 54, the pre-detection integration circuitry 56 and the correlator switches 58 shown in the typical C/A- and P-code channel 37 of FIGURE 2. The only difference being that there is an extra set of P-code delay shift registers 78, P-code mixers 92 and correlator switches 100 and that the pre-detection integration circuitry 332 supports three additional correlators. This is done to accommodate the extra three correlators required to track L2 P-code.

Unique to the enhanced channel is a modified P-code clock generator 62, a P-code circular buffer 66, two P-code chip counters, 68 and 72, and two 16-to-1 multiplexers (MUX), 70 and 74.

FIGURE 4 shows a high level block diagram of the modified P-code clock generator 62. This circuit is a unique modification of the low-powered digital oscillator detailed in co-pending application entitled "Method and Systems for a Multi-Channel Global Position System Signal Processor", published as EP0 501 828. Circuitry to determine which clock leads is not shown. One approach to determine the leading clock is to extend the P-code chip counters 68 and 74 an extra two bits and compare the counter values to see which clock leads.

The circuit operation of the modified P-code clock generator 62, is basically the same as the code clock generator described in the previously mentioned co-pending U.S. Patent Applications. The modification is that there are two separate 16-bit P-code clock phase words 112 and 114, one for determining the phase of the L1 P-code clock and the other for determining the phase of the L2 P-code clock. Since initial P-code clock phase only affects the 13 most significant bits of the 32-bit P-code clock generator adder/accumulator, the 19 least significant bits of the adder/accumulator 122 are common to both the L1 and the L2 P-code clock. The frequency word 116 is also common to both the L1 and L2 P-code clock. Along with the two separate P-code clock

phase words, 112 and 114 are two 13-bit adder/accumulators 118 and 120 one for L1 P-code clock and one for L2 P-code clock, which together with the 19-bit adder/accumulator 122 make up two separate 32-bit adder/accumulators capable of generating carriers to the two state machines 124 and 126 with the same frequency but different phase. The state machine and carry delay circuits 124 and 126 are exactly the same as described in the previously mentioned co-pending U.S. Patent Applications.

FIGURE 5 shows the estimated difference between a typical single L-band channel and the enhanced L1/L2 channel of the present invention. An enhanced channel requires only 42% additional circuitry over a normal channel and provides the performance benefit and software reduction of two completely independent channels for tracking L1 and L2 simultaneously.

The cost of the enhanced channel is considerably less than the 42% when overhead circuitry such as channel timing and control, processor interface and search specific circuits are included in the gate count estimates. Also note that for this specific example, that the enhanced channel has three additional correlators. This provides approximately a 50% improvement in search speed. As a result of the enhanced P-code channel of the present invention, there is provided an apparatus and method for significantly increasing GPS system receiver channel flexibility without a significant increase in circuitry or software complexity.

Although this description describes the invention with reference to the above specific embodiments, the claims, and not this description, limit the scope of the invention. Various modifications or the disclosed embodiment, as well as alternative embodiments of the invention, will become apparent to persons skilled in the art upon reference to the above description. Therefore, the appended claims will cover such modification that follow up in the true scope of the invention.

Aspects of the present invention will be further appreciated from the following:

The P-Code Channel on-a-chip (PCOAC) to be described is a dual channel GPS signal processor integrated circuit. A 95-pin ceramic pin-grid-array (PGA) contains the 348,300 transistor CMOS gate array. Major features include: two independent GPS channels; a search processor for improved acquisition time; an embedded Y-code generator; system synchronization control; and a 16-bit processor interface.

Figure 6 shows a block diagram of PCOAC 1010. Unused functions can be turned off allowing for a high level of power conservation in applications where power usage and/or heat dissipation is an important consideration.

Each channel of circuit 1010 is a dedicated signal processing circuit which de-modulates the code and carrier of a GPS signal and performs pre-detection integration. Each channel contains a code clock generator 1103 (1104), a P and C/A-code generator 1105 (1106),

an L1/L2 carrier generator 1109 (1110), eight correlators 1111, 1113, 1115, 1117 (1112, 1114, 1116, 1118) and a noise meter 1119 (1120). Each of the eight correlators can be selected to operate with C/A-code or P-Code. A Y-code generator 1108 common to both channels provides independent Y-code for both channels.

Search processor 1123 and discrete fourier transform (DFT) function 1124 improve signal acquisition capability. The DFT separates the sample integration data into seven frequency bins. Search processor 1123 interpolates between these seven frequency bins to obtain six additional frequency bins, producing a total of thirteen frequency bins per correlator. The search processor implements a Tong detection algorithm on all eight correlators for each of the thirteen frequency bins resulting in the simultaneous search of 1104 search bins per channel.

PCOAC 1010 supports three frequency plans, 57.7920 MHz, 40.9216 MHz and 40.9200 MHz operation. Several programmable clocks/interrupts 1130 are provided to synchronize the host processor to PCOAC operation. Various interrupt schemes are designed to allow trade-offs to be made between system performance, processor throughput requirements and the complexity of the software.

A standard 16-bit processor interface 1131 is utilized. In order to minimize read/write overhead to the PCOAC, integration samples are buffered 1121 (1122) and the memory map is designed so that block moves are all that is required for channel updates during normal tracking operations.

Figure 7 is a block diagram of the top level modules which electrically make up channel A(11) of PCOAC 10. Base Band Module 1130 generates several global clocks for system synchronization;

Channel Timing Module 1101 generates all clocks and synchronization pulses specific to a single channel;

Code Generator Module 21 includes a programmable code clock generator, P-code and C/A-code generators/setters, and P-code and C/A-code state advance and retard for search;

Y-Code Generator Module 1108 converts the P-code into Y-code for both channels simultaneously even during code state advances;

Front-End Correlator Module 1201 provides L1 or L2 carrier generation, a carrier mixer, a P-code and C/A-code delay shift register (to generate eight code phases), code mixers, data wipe-off, and noise meter signal selection;

Intermediate Correlator Module 1202 performs the first stage of sample integration for eight complex

correlators and a noise meter;

Back-End Correlator Module 1203 performs the final stage of sample integration, and also performs noise measurement for aiding in search and tracking (one per channel);

I RAM 1204 and Q RAM 1205 are two 64 x 16-bit 3-port RAMs per channel for sample integration buffering or to hold intermediate values for DFT calculations;

Discrete Fourier Transform (DFT) Module 1124 converts integration samples from all correlators of both channels into seven frequency bins of sample data for search operations;

Search Processor Module 1206 interpolates six additional frequency bins from those provided by the DFT module, performs Tong detection on all thirteen frequency bins of data and retards the code state until a signal is found;

Search Processor RAM 1207 is a 64 x 16-bit 3-port RAM used by the search processor as a holding register for active Tong counts during search or noise measurement buffering during tracking;

Processor Interface Module 1131 provides address decode to generate internal read and write strobes, integration sample buffering control, a programmable ring oscillator for test and other miscellaneous functions.

Digital signal processing circuitry as exemplified herein may be implemented by means of a single integrated circuit.

## Claims

1. An enhanced precision code (P-code) channel (60) for use in a GPS receiver, the said channel (60) being capable of simultaneously tracking first and second band signals (L1,L2) and comprising:

circuitry (64,66) for generating P-code signals and storing the most recently generated of said P-code signals;

a first circuit (68, 70) for selecting and updating first P-code signals having a first phase from said P-code signals, said selected and updated first P-code signals being in-phase with a first code clock associated with the first band signal (L1);

a second circuit (72, 74) for selecting and updating second P-code signals having a second phase from said P-code signals, said selected and updated second P-code signals being in-phase with a second code clock associated

with the second band signal (L2); and  
a P-code clock generator (62) for generating said first code clock, the first and second code clocks having the same frequency but different phase;

characterised in that:

said P-code clock generator (62) is capable of simultaneously generating the second code clock and said circuitry (64,66) is capable of generating a plurality of P-code signals each having a different phase.

2. A signal processor for use in a GPS receiver including:

digital signal processing circuitry (26, 28, 30) for acquiring and tracking P-code signals from at least one satellite of a GPS system; and  
an enhanced precision code (P-code) channel (60), the said channel (60) being capable of simultaneously tracking first and second band signals (L1,L2) and comprising:

circuitry (64,66) for generating P-code signals and storing the most recently generated of said P-code signals;

a first circuit (68, 70) for selecting and updating first P-code signals having a first phase from said P-code signals, said selected and updated first P-code signals being in-phase with a first code clock associated with the first band signal (L1);

a second circuit (72, 74) for selecting and updating second P-code signals having a second phase from said P-code signals, said selected and updated second P-code signals being in-phase with a second code clock associated with the second band signal (L2); and

a P-code clock generator (62) for generating said first code clock, the first and second code clocks having the same frequency but different phase;

characterised in that:

said P-code clock generator (62) is capable of simultaneously generating the second code clock and said circuitry (64,66) is capable of generating a plurality of P-code signals each having a different phase.

3. A receiver (10) for determining the position of at least one satellite of a GPS system, the receiver (10) comprising;

a digital processing circuit (26, 28, 30) for acquiring a signal from the or each one satellite in the presence of noise, and generating an estimate of the current position of the or each satellite based upon data exchanged between the digital signal

processing circuit (26, 28, 30) and a signal processor, said signal processor including:  
 an enhanced precision code (P-code) channel (60), the said channel (60) being capable of simultaneously tracking first and second band signals (L1, L2) and comprising:

circuitry (64, 66) for generating P-code signals and storing the most recently generated of said P-code signals;

a first circuit (68, 70) for selecting and updating first P-code signals having a first phase from said P-code signals, said selected and updated first P-code signals being in-phase with a first code clock associated with the first band signal (L1);

a second circuit (72, 74) for selecting and updating second P-code signals having a second phase from said P-code signals, said selected and updated second P-code signals being in-phase with a second code clock associated with the second band signal (L2); and

a P-code clock generator (62) for generating said first code clock, the first and second code clocks having the same frequency but different phase;

characterised in that:

said P-code clock generator (62) is capable of simultaneously generating the second code clock and said circuitry (64, 66) is capable of generating a plurality of P-code signals each having a different phase.

4. Apparatus according to any one of Claims 1 - 3, characterised in that the apparatus further comprises;

a P-code circular buffer (302) within the generating and storing circuitry (64, 66), the circular buffer (302) being adapted to generate two phases of P-code signal for tracking the first and second band signals (L1, L2).

5. Apparatus according to any one of Claims 1 - 4, characterised in that the apparatus independently tracks either the first or second band signal (L1, L2).

6. Apparatus according to any one of Claims 2 - 5, characterised in that the apparatus further comprises circuitry (44, 46, 62) for simultaneously generating a coarse-acquisition code (C/A code) for the first band signal (L1), the precision-code (P-code) for the first band signal (L1), and the P-code for the second band signal (L2).

7. Apparatus according to any one of Claims 2-6, characterised in that the apparatus further comprises circuitry (56, 96, 332) for vector summing said C/A

code for the first band signal (L1), the P-code for the first band signal (L1), and the P-code for the second band signal

8. Apparatus according to any one of Claims 2 - 7, characterised in that the apparatus further comprises circuitry for continuous ionospheric correction within said channel (60).

9. Apparatus according to any one of Claims 2 - 8, characterised in that the or each satellite is a navigational satellite.

10. A method for simultaneously tracking first and second band signals (L1, L2) in a P-code channel (60) for use in a GPS receiver, the method comprising:

generating P-code signals and storing a plurality of the most recently generated of said P-code signals;

selecting and updating first P-code signals having a first phase from the stored plurality of P-code signals in-phase with a first code clock associated with the first band signal (L1);

selecting and updating second P-code signals having a second phase from the stored plurality of P-code signals in-phase with a second code clock associated with the second band signal (L2); and

generating said first P-code clock using a P-code generator (64), the code clocks having the same frequency but different phase,

characterised in that said second P-code clock is generated simultaneously with said first P-code clock and in that a plurality of P-code signals are generated each having a different phase.

11. The method according to Claim 10, characterised in that the method further comprises ;

tracking the first band signal (L1) in the channel (60) for assisting second band signal (L2) tracking.

12. The method according to Claim 10, characterised in that the method further comprises;

tracking the second band signal (L2) in the channel (60) for assisting first band signal (L1) tracking.

13. The method according to any one of Claims 10 - 12, characterised in that the method further comprises;

generating two phases of P-code for tracking the first and second band signals (L1, L2) separately.

14. The method according to any one of Claims 10 - 12, characterised in that the method further comprises;

independently tracking either the first or second band signal (L1, L2).

15. The method according to any one of Claims 10 - 14, characterised in that the method further comprises; 5  
simultaneously generating a C/A-code for the first band signal (L1), P-code for the first band signal (L1), and the P-code for the second band signal (L2) within said enhanced P-code channel (60). 10
16. The method according to Claim 15, characterised in that the method further comprises;  
vector summing said C/A-code for the first band signal (L1), P-code for the first band signal (L1), and the P-code for the second band signal (L2). 15

#### Patentansprüche

1. Verbesserter Präzisionscode-Kanal (P-Code-Kanal) (60) für die Verwendung in einem GPS-Empfänger, wobei der Kanal (60) gleichzeitig ein erstes und ein zweites Bandsignal (L1, L2) verfolgen kann und enthält; 20  
  
eine Schaltung (64, 66) zum Erzeugen von P-Code-Signalen und zum Speichern der zuletzt erzeugten P-Code-Signale;  
eine erste Schaltung (68, 70) zum Auswählen und Aktualisieren erster P-Code-Signale mit einer ersten Phase aus den P-Code-Signalen, wobei die ausgewählten und aktualisierten ersten P-Code-Signale mit einem ersten Code-Takt, der dem ersten Bandsignal (L1) zugeordnet ist, in Phase sind; 30  
eine zweite Schaltung (72, 74) zum Auswählen und Aktualisieren zweiter P-Code-Signale mit einer zweiten Phase aus den P-Code-Signalen, wobei die ausgewählten und aktualisierten zweiten P-Code-Signale mit einem zweiten Code-Takt, der dem zweiten Bandsignal (L2) zugeordnet ist, in Phase sind; und 35  
einen P-Code-Taktgenerator (62) zum Erzeugen des ersten Code-Takts, wobei der erste und der zweite Code-Takt die gleiche Frequenz, jedoch unterschiedliche Phase besitzen; dadurch gekennzeichnet, daß:  
der P-Code-Taktgenerator (62) gleichzeitig den zweiten Code-Takt erzeugen kann und die Schaltung (64, 66) mehrere P-Code-Signale erzeugen kann, wovon jedes eine unterschiedliche Phase besitzt. 40  
45
2. Signalprozessor für die Verwendung in einem GPS-Empfänger, mit: 55  
  
einer digitalen Signalverarbeitungsschaltung

(26, 28, 30) für die Erfassung und Verfolgung von P-Code-Signalen von wenigstens einem Satelliten eines GPS-Systems; und einem verbesserten Präzisionscode-Kanal (P-Code-Kanal) (60), wobei der Kanal (60) gleichzeitig ein erstes und ein zweites Bandsignal (L1, L2) verfolgen kann und enthält:  
eine Schaltung (64, 66) zum Erzeugen von P-Code-Signalen und zum Speichern der zuletzt erzeugten P-Code-Signale;  
eine erste Schaltung (68, 70) zum Auswählen und Aktualisieren erster P-Code-Signale mit einer ersten Phase aus den P-Code-Signalen, wobei die ausgewählten und aktualisierten ersten P-Code-Signale mit einem ersten Code-Takt, der dem ersten Bandsignal (L1) zugeordnet ist, in Phase sind;  
eine zweite Schaltung (72, 74) zum Auswählen und Aktualisieren zweiter P-Code-Signale mit einer zweiten Phase aus den P-Code-Signalen, wobei die ausgewählten und aktualisierten zweiten P-Code-Signale mit einem zweiten Code-Takt, der dem zweiten Bandsignal (L2) zugeordnet ist, in Phase sind; und  
einen P-Code-Taktgenerator (62) zum Erzeugen des ersten Code-Takts, wobei der erste und der zweite Code-Takt die gleiche Frequenz, jedoch unterschiedliche Phase besitzen; dadurch gekennzeichnet, daß:  
der P-Code-Taktgenerator (62) gleichzeitig den zweiten Code-Takt erzeugen kann und die Schaltung (64, 66) mehrere P-Code-Signale erzeugen kann, wovon jedes eine andere Phase besitzt.

3. Empfänger (10) für die Bestimmung der Position wenigstens eines Satelliten eines GPS-Systems, wobei der Empfänger (10) enthält;

eine digitale Verarbeitungsschaltung (26, 28, 30) für die Erfassung eines Signals von dem oder jedem Satelliten bei Vorhandensein von Rauschen und zum Erzeugen einer Schätzung der momentanen Position des oder jedes Satelliten auf der Grundlage von Daten, die zwischen der digitalen Signalverarbeitungsschaltung (26, 28, 30) und einem Signalprozessor ausgetauscht werden, wobei der Signalprozessor enthält:  
eine Schaltung (64, 66) zum Erzeugen von P-Code-Signalen und zum Speichern der zuletzt erzeugten P-Code-Signale;  
eine erste Schaltung (68, 70) zum Auswählen und Aktualisieren erster P-Code-Signale mit einer ersten Phase aus den P-Code-Signalen, wobei die ausgewählten und aktualisierten ersten P-Code-Signale mit einem ersten Code-Takt, der dem ersten Bandsignal (L1) zugeordnet

net ist, in Phase sind;  
 eine zweite Schaltung (72, 74) zum Auswählen und Aktualisieren zweiter P-Code-Signale mit einer zweiten Phase aus den P-Code-Signalen, wobei die ausgewählten und aktualisierten zweiten P-Code-Signale mit einem zweiten Code-Takt, der dem zweiten Bandsignal (L2) zugeordnet ist, in Phase sind; und  
 einen P-Code-Taktgenerator (62) zum Erzeugen des ersten Code-Takts, wobei der erste und der zweite Code-Takt die gleiche Frequenz, jedoch unterschiedliche Phase besitzen; dadurch gekennzeichnet, daß:  
 der P-Code-Taktgenerator (62) gleichzeitig den zweiten Code-Takt erzeugen kann und die Schaltung (64, 66) mehrere P-Code-Signale erzeugen kann, wovon jedes eine unterschiedliche Phase besitzt.

4. Vorrichtung nach irgendeinem der Ansprüche 1-3, dadurch gekennzeichnet, daß sie ferner enthält:  
 einen P-Code-Zirkulärpuffer (302) in der Erzeugungs- und Speicherschaltung (64, 66), wobei der Zirkulärpuffer (302) so beschaffen ist, daß er zwei Phasen des P-Code-Signals für die Verfolgung des ersten und des zweiten Bandsignals (L1, L2), erzeugt.
5. Vorrichtung nach irgendeinem der Ansprüche 1-4 dadurch gekennzeichnet, daß die Vorrichtung das erste und das zweite Bandsignal (L1, L2) unabhängig voneinander verfolgt.
6. Vorrichtung nach irgendeinem der Ansprüche 2-5, dadurch gekennzeichnet, daß die Vorrichtung ferner eine Schaltung (44, 46, 62) zum gleichzeitigen Erzeugen eines Kurserfassungs-codes (C/A-Code) für das erste Bandsignal (L1), des Präzisions-codes (P-Code) für das erste Bandsignal (L1) und des P-Codes für das zweite Bandsignal (L2) enthält.
7. Vorrichtung nach irgendeinem der Ansprüche 2-6, dadurch gekennzeichnet, daß die Vorrichtung ferner eine Schaltung (56, 96, 332) für die Vektoraddition des C/A-Codes für das erste Bandsignal (L1), des P-Codes für das erste Bandsignal (L1) und des P-Codes für das zweite Bandsignal enthält.
8. Vorrichtung nach irgendeinem der Ansprüche 2-7, dadurch gekennzeichnet, daß die Vorrichtung ferner eine Schaltung für die kontinuierliche ionosphärische Korrektur in dem Kanal (60) enthält.
9. Vorrichtung nach irgendeinem der Ansprüche 2-8, dadurch gekennzeichnet, daß der oder jeder Satellit ein Navigationssatellit ist.
10. Verfahren zum gleichzeitigen Verfolgen erster und

zweiter Bandsignale (L1, L2) in einem P-Code-Kanal (60) für die Verwendung in einem GPS-Empfänger, wobei das Verfahren enthält:

- 5 Erzeugen von P-Code-Signalen und Speichern mehrerer der zuletzt erzeugten P-Code-Signale;  
 Auswählen und Aktualisieren erster P-Code-Signale mit einer ersten Phase aus den gespeicherten mehreren P-Code-Signalen, die mit einem ersten Code-Takt, der dem ersten Bandsignal (L1) zugeordnet ist, in Phase sind;  
 Auswählen und Aktualisieren zweiter P-Code-Signale mit einer zweiten Phase aus den gespeicherten mehreren P-Code-Signalen, die mit einem zweiten Code-Takt, der dem zweiten Bandsignal (L2) zugeordnet ist, in Phase sind; und  
 Erzeugen des ersten P-Code-Takts unter Verwendung eines P-Code-Generators (64), wobei die Code-Takte die gleiche Frequenz, jedoch unterschiedliche Phase besitzen, dadurch gekennzeichnet, daß der zweite P-Code-Takt gleichzeitig mit dem ersten P-Code-Takt erzeugt wird und daß mehrere der P-Code-Signale erzeugt werden, wovon jedes eine unterschiedliche Phase besitzt.
11. Verfahren nach Anspruch 10, dadurch gekennzeichnet, daß das Verfahren ferner enthält:  
 Verfolgen des ersten Bandsignals (L1) im Kanal (60), um die Verfolgung des zweiten Bandsignals (L2) zu unterstützen.
12. Verfahren nach Anspruch 10, dadurch gekennzeichnet, daß das Verfahren ferner enthält:  
 Verfolgen des zweiten Bandsignals (L2) im Kanal (60), um die Verfolgung des ersten Bandsignals (L1) zu unterstützen.
13. Verfahren nach irgendeinem der Ansprüche 10-12, dadurch gekennzeichnet, daß das Verfahren ferner enthält:  
 Erzeugen zweier Phasen des P-Codes zum getrennten Verfolgen der ersten und zweiten Bandsignale (L1, L2).
14. Verfahren nach irgendeinem der Ansprüche 10-12, dadurch gekennzeichnet, daß das Verfahren ferner enthält:  
 unabhängiges Verfolgen entweder des ersten oder des zweiten Bandsignals (L1, L2).
15. Verfahren nach irgendeinem der Ansprüche 10-14, dadurch gekennzeichnet, daß das Verfahren ferner enthält:  
 gleichzeitiges Erzeugen eines C/A-Codes für das erste Bandsignal (L1), eines P-Codes für das



erste Bandsignal (L1) und des P-Codes für das zweite Bandsignal (L2) im verbesserten P-Code-Kanal (60).

16. Verfahren nach Anspruch 15, dadurch gekennzeichnet, daß das Verfahren ferner enthält:  
 ein vektorielles Addieren des C/A-Codes für das erste Bandsignal (L1), des P-Codes für das erste Bandsignal (L1) und des P-Codes für das zweite Bandsignal (L2).

## Revendications

1. Voie à code de précision (code P) amélioré (60) pour un récepteur de système de positionnement global (GPS), ladite voie (60) étant capable d'assurer simultanément la poursuite d'un premier et d'un deuxième signal de bande (L1, L2) et comprenant :  
 un circuit (64, 66) destiné à générer des signaux à code P et à stocker les signaux le plus récemment générés desdits signaux à code P ;  
 un premier circuit (68, 70) destiné à sélectionner et à mettre à jour des premiers signaux à code P ayant une première phase parmi lesdits signaux à code P, lesdits premiers signaux à code P sélectionnés et mis à jour étant en phase avec une première impulsion d'horloge à code associée au premier signal de bande (L1) ;  
 un deuxième circuit (72, 74) destiné à sélectionner et à mettre en jour des deuxièmes signaux à code P ayant une deuxième phase parmi lesdits signaux à code P, lesdits deuxièmes signaux à code P sélectionnés et mis à jour étant en phase avec une deuxième impulsion d'horloge à code associée au deuxième signal de bande (L2) ; et  
 un générateur d'impulsions d'horloge à code P (62) destiné à générer ladite première impulsion d'horloge à code, les première et deuxième impulsions d'horloge à code ayant la même fréquence mais une phase différente ; caractérisée en ce que ;  
 ledit générateur d'impulsions d'horloge à code P (62) est capable de générer simultanément la deuxième impulsion d'horloge à code et ledit circuit (64, 66) est capable de générer une pluralité de signaux à code P ayant chacun une phase différente.
2. Dispositif de traitement de signal pour un récepteur de système de positionnement global comprenant :  
 un circuit de traitement numérique de signal (26, 28, 30) destiné à assurer l'acquisition et la poursuite de signaux à code P provenant d'au moins un satellite d'un système de positionne-

ment global ; et

une voie à code de précision (code P) amélioré (60), ladite voie (60) étant capable d'assurer simultanément la poursuite d'un premier et d'un deuxième signal de bande (L1, L2) et comprenant :

un circuit (64, 66) destiné à générer des signaux à code P et à stocker les signaux le plus récemment générés desdits signaux à code P ;  
 un premier circuit (68, 70) destiné à sélectionner et à mettre à jour des premiers signaux à code P ayant une première phase parmi lesdits signaux à code P, lesdits premiers signaux à code P sélectionnés et mis à jour étant en phase avec une première impulsion d'horloge à code associée au premier signal de bande (L1) ;  
 un deuxième circuit (72, 74) destiné à sélectionner et à mettre à jour des deuxièmes signaux à code P ayant une deuxième phase parmi lesdits signaux à code P, lesdits signaux à code P sélectionnés et mis à jour étant en phase avec une deuxième impulsion d'horloge à code associée au deuxième signal de bande (L2) ; et  
 un générateur d'impulsions d'horloge à code P (62) destiné à générer ladite première impulsion d'horloge à code, les première et deuxième impulsions d'horloge à code ayant la même fréquence mais une phase différente ; caractérisé en ce que :  
 ledit générateur d'impulsions d'horloge à code P (62) est capable de générer simultanément la deuxième impulsion d'horloge à code et ledit circuit (64, 66) est capable de générer une pluralité de signaux à code P ayant chacun une phase différente.

3. Récepteur (10) destiné à déterminer la position d'au moins un satellite d'un système de positionnement global, le récepteur (10) comprenant :  
 un circuit de traitement numérique (26, 28, 30) destiné à assurer l'acquisition d'un signal provenant du satellite ou de chaque satellite en présence de bruit, et à générer une estimation de la position courante du satellite ou de chaque satellite sur la base des données échangées entre le circuit de traitement numérique de signal (26, 28, 30) et un dispositif de traitement de signal, ledit dispositif de traitement du signal comprenant :

une voie à code de précision (code P) amélioré (60), ladite voie (60) étant capable d'assurer simultanément la poursuite d'un premier et d'un deuxième signal de bande (L1, L2) et comprenant :

un circuit (64, 66) destiné à générer des signaux à code P et à stocker les signaux le plus récemment générés desdits signaux à code P ;

- un premier circuit (68, 70) destiné à sélectionner et à mettre à jour des premiers signaux à code P ayant une première phase parmi lesdits signaux à code P, lesdits premiers signaux à code P sélectionnés et mis à jour étant en phase avec une première impulsion d'horloge à code associée au premier signal de bande (L1); un deuxième circuit (72, 74) destiné à sélectionner et à mettre à jour des deuxièmes signaux à code P ayant une deuxième phase parmi lesdits signaux à code P, lesdits signaux à code P sélectionnés et mis à jour étant en phase avec une deuxième impulsion d'horloge à code associée au deuxième signal de bande (L2); et un générateur d'impulsions d'horloge à code P (62) destiné à générer ladite première impulsion d'horloge à code, les première et deuxième impulsions d'horloge à code ayant la même fréquence mais une phase différente; caractérisé en ce que; ledit générateur d'impulsions d'horloge à code P (62) est capable de générer simultanément la deuxième impulsion d'horloge à code et ledit circuit (64, 66) est capable de générer une pluralité de signaux à code P ayant chacun une phase différente.
4. Appareil selon l'une quelconque des revendications 1 à 3, caractérisé en ce que l'appareil comprend en outre;
    - un circuit tampon circulaire à code P (302) dans le circuit de génération et de stockage (64, 66), le circuit tampon circulaire (302) étant adapté pour générer deux phases de signal à code P pour la poursuite des premier et deuxième signaux de bande (L1, L2).
  5. Appareil selon l'une quelconque des revendications 1 à 4, caractérisé en ce que l'appareil assure indépendamment la poursuite du premier ou du deuxième signal de bande (L1, L2).
  6. Appareil selon l'une quelconque des revendications 2 à 5, caractérisé en ce que l'appareil comprend en outre un circuit (44, 46, 62) destiné à générer simultanément un code d'acquisition approchée (code C/A) pour le premier signal de bande (L1), le code de précision (code P) pour le premier signal de bande (L1) et le code P pour le deuxième signal de bande (L2).
  7. Appareil selon l'une quelconque des revendications 2 à 6, caractérisé en ce que l'appareil comprend en outre un circuit (56, 96, 332) destiné à faire la somme vectorielle dudit code C/A pour le premier signal de bande (L1), du code P pour le premier signal de bande (L1) et du code P pour le deuxième signal de bande.
  8. Appareil selon l'une quelconque des revendications 2 à 7, caractérisé en ce que l'appareil comprend en outre un circuit destiné à assurer la correction ionosphérique continue dans ladite voie (60).
  9. Appareil selon l'une quelconque des revendications 2 à 8, caractérisé en ce que le satellite ou chaque satellite est un satellite de navigation.
  10. Procédé pour assurer simultanément la poursuite de premier et deuxième signaux de bande (L1, L2) dans une voie à code P (60) pour un récepteur de système de positionnement global, le procédé comprenant:
    - la génération de signaux à code P et le stockage d'une pluralité des signaux le plus récemment générés desdits signaux à code P;
    - la sélection et la mise à jour de premiers signaux à code P ayant une première phase parmi la pluralité stockée de signaux à code P en phase avec une première impulsion d'horloge à code associée au premier signal de bande (L1);
    - la sélection et la mise à jour de deuxièmes signaux à code P ayant une deuxième phase parmi la pluralité stockée de signaux à code P en phase avec une deuxième impulsion d'horloge à code associée au deuxième signal de bande (L2); et
    - la génération de ladite première impulsion d'horloge à code P en utilisant un générateur à code P (64), les impulsions d'horloge à code ayant la même fréquence mais une phase différente, caractérisé en ce que ladite deuxième impulsion d'horloge à code P est générée simultanément à ladite première impulsion d'horloge à code P et en ce que plusieurs signaux à code P sont générés ayant chacun une phase différente.
  11. Procédé selon la revendication 10, caractérisé en ce que le procédé comprend en outre:
    - la poursuite du premier signal de bande (L1) dans la voie (60) pour faciliter la poursuite du deuxième signal de bande (L2).
  12. Procédé selon la revendication 10, caractérisé en ce que le procédé comprend en outre:
    - la poursuite du deuxième signal de bande (L2) dans la voie (60) pour faciliter la poursuite du premier signal de bande (L1).
  13. Procédé selon l'une quelconque des revendications 10 à 12, caractérisé en ce que le procédé comprend en outre le fait de:

générer deux phases de code P pour la poursuite des premier et deuxième signaux de bande (L1, L2) séparément.

14. Procédé selon l'une quelconque des revendications 10 à 12, caractérisé en ce que le procédé comprend en outre :  
la poursuite du premier ou du deuxième signal de bande (L1, L2) indépendamment. 5  
10
15. Procédé selon l'une quelconque des revendications 10 à 14, caractérisé en ce que le procédé comprend en outre le fait de :  
générer simultanément un code C/A pour le premier signal de bande (L1), le code P pour le premier signal de bande (L1) et le code P pour le deuxième signal de bande (L2) dans ladite voie à code P amélioré (60). 15  
20
16. Procédé selon la revendication 15, caractérisé en ce que le procédé comprend en outre le fait de :  
faire la somme vectorielle dudit code C/A pour le premier signal de bande (L1), du code P pour le premier signal de bande (L1) et du code P pour le deuxième signal de bande (L2). 25

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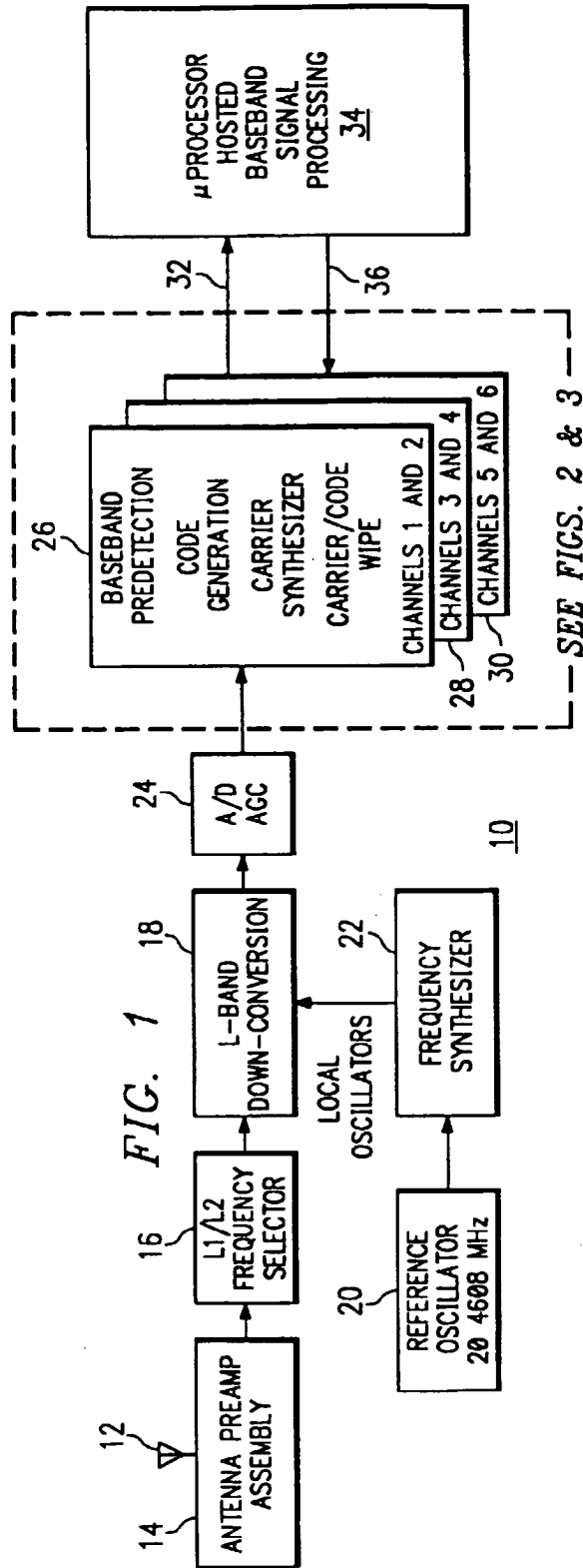
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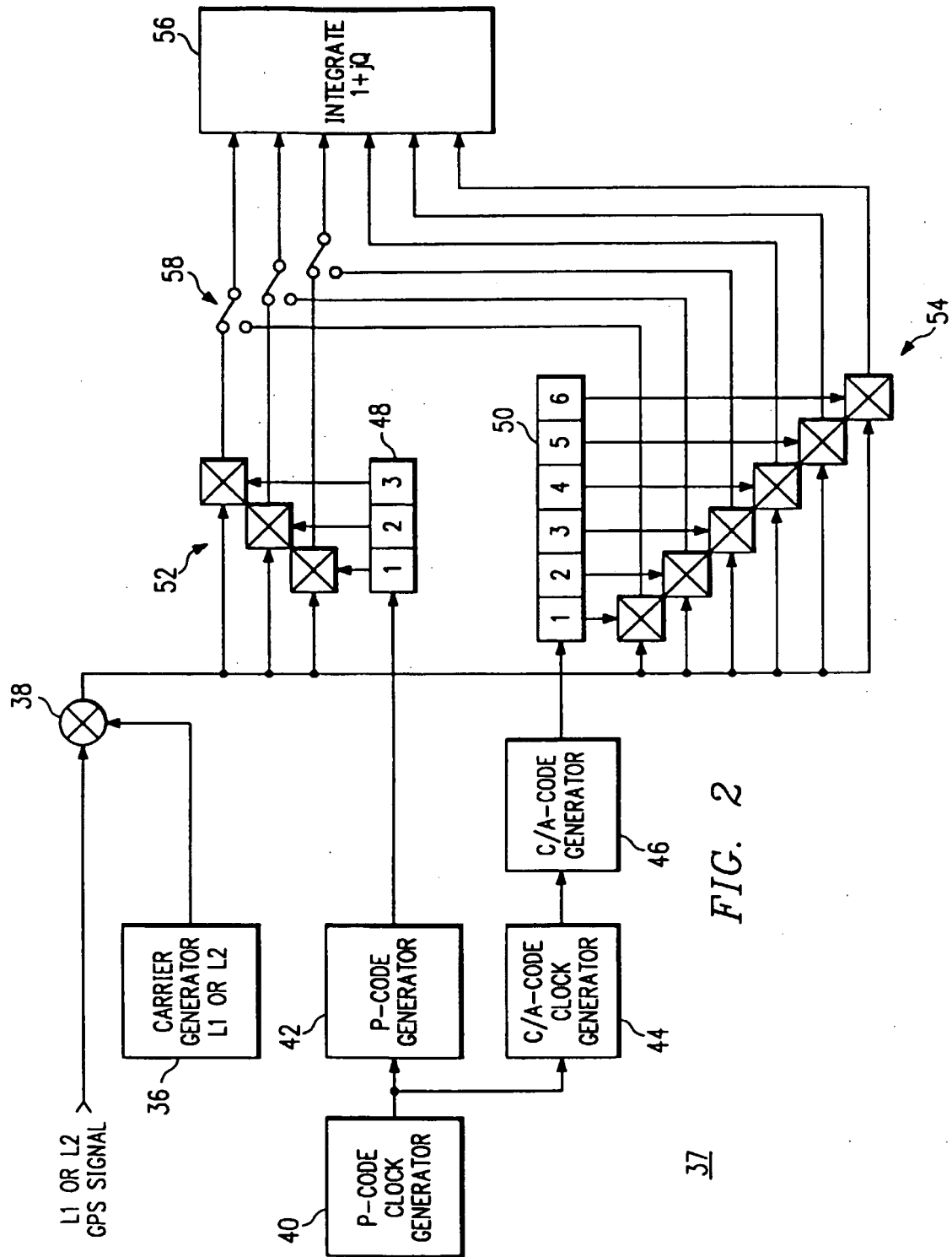
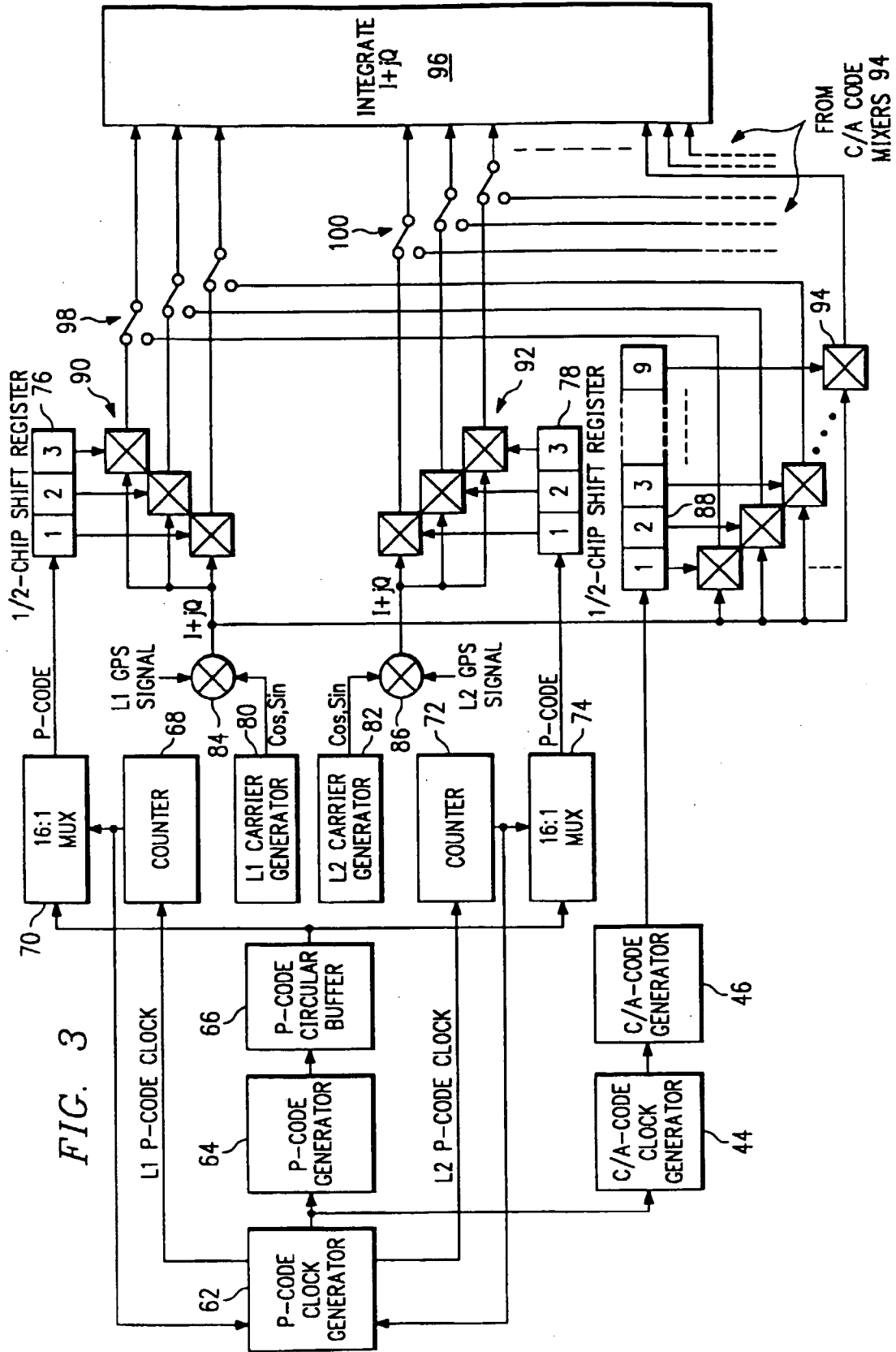


FIG. 2



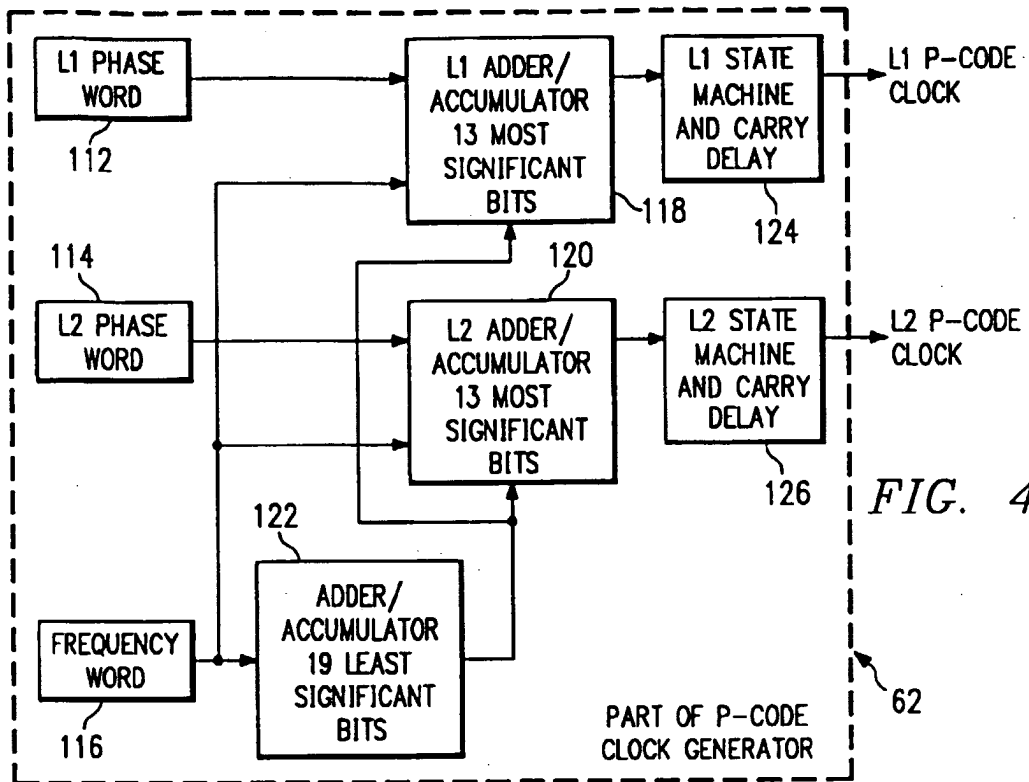
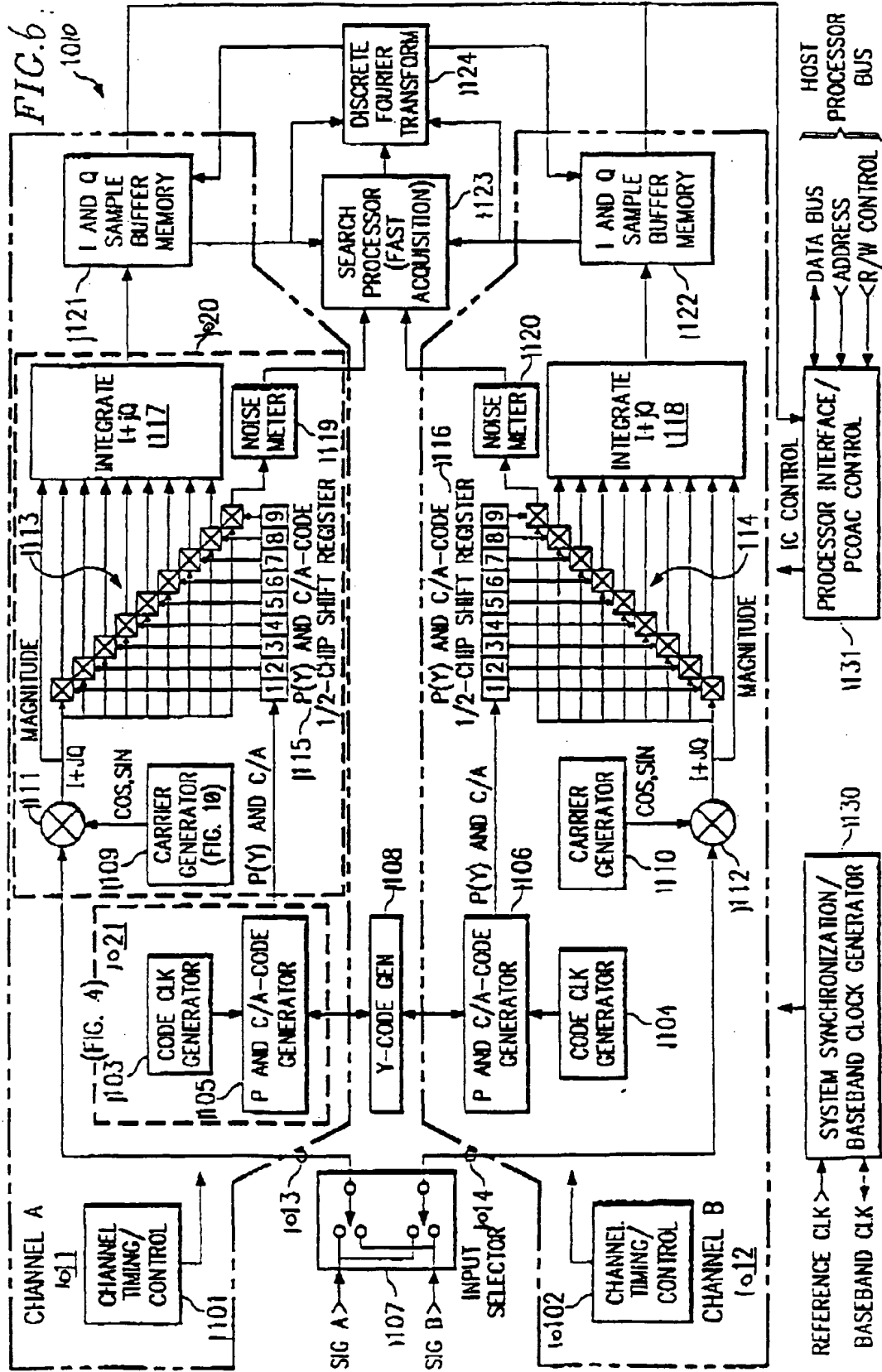


FIG. 4

FIG. 5 GATE COUNT OF PRIOR ART CHANNEL VERSUS ENHANCED L1/L2 CHANNEL

FUNCTION	TYPICAL		ENHANCED	
	QTY	GATES	QTY	GATES
CARRIER GENERATOR 36,80,82	1	1244	2	2488
CARRIER MIXER 38,84,86	1	126	2	252
P-CODE CLOCK GEN. 40,62	1	1246	1.5	1869
P-CODE GENERATOR 42,64	1	3000	1	3000
CIRCULAR BUFFER 66	0	0	1	150
COUNTER 68,72	0	0	2	60
16:1 MULTIPLEXER 70,74	0	0	2	66
P-CODE DELAY SHIFT REG. 48,76,78	1	25	2	50
P-CODE MIXERS 52,90,92	3	9	6	18
C/A-CODE CLOCK GEN. 44	1	50	1	50
C/A-CODE GEN. 46	1	500	1	500
C/A-CODE DELAY SHIFT REG. 50,88	1	50	1	75
C/A-CODE MIXERS 54,94	6	18	9	27
CORRELATOR SWITCH 58,98,100	3	9	6	18
INTEGRATORS 56,96	6	4100	9	6150
TOTAL		10,377		14,773





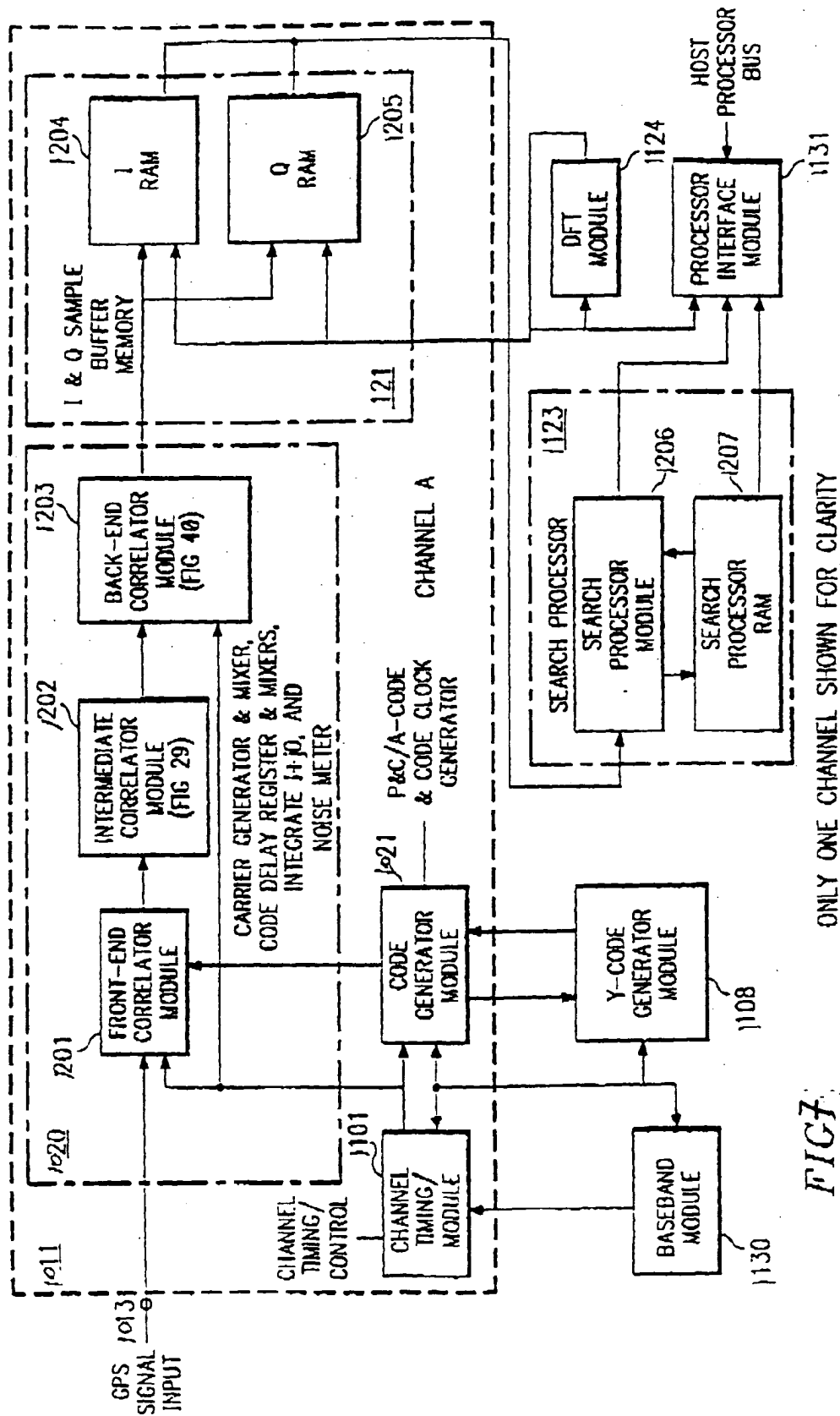


FIG. 1 ONLY ONE CHANNEL SHOWN FOR CLARITY